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TRX_120_067

120-GHz Highly Integrated IQ Transceiver with Antennas in Package
in Silicon Germanium Technology

Data Sheet

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Data Sheet

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Version Control

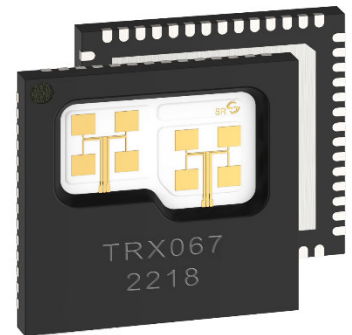
Version	Changed section	Description of change
0.1	Template, contents	Initial release
0.2	8 Measurement Results	Scale in figures 20 and 21 corrected
0.3	6.3 Evaluation Kit	Information regarding to SR's new SiRad Easy® r4 platform
0.4	4.4 Electrical Characteristics 7 Reliability and Environmental Test	Notation of 'IQ amplitude imbalance' (Aimb) notation corrected. Status of all tests listed in Table 7 updated.
0.5	5.1 Outline Dimensions 8 Measurement Results	Figure 4, Position of Antenna Arrays... : Mold cap dimension corrected, and cross section added. Figure 8, Current Consumption vs. Temperature, and figure 16, TX Output Frequency vs. Temperature: shown temperature range extended.
1.0	4.4 Electrical Characteristics 7 Reliability and Environmental Test	Start and Stop Frequency limits changed to include latest test statistics. EIRP value added. All tests listed in Table 7 completed and passed.
1.1	4.4 Electrical Characteristics All sections	Update with data from serial test. Minor corrections to remove typos.

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1 Features

- Radar front end (RFE) with antennas in package for 122-GHz ISM band
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 380 mW in continuous operating mode
- Duty cycling is possible
- Integrated low phase noise push-push VCO
- Receiver with homodyne quadrature mixer
- RX and TX patch antennas
- Wide bandwidth of up to 6 GHz
- QFN56 leadless plastic package $8 \times 8 \text{ mm}^2$
- Package partly molded, MSL3 rated
- Pb-free, RoHS compliant package
- Replaces the TRX_120_001



1.1 Overview

The RFE is an integrated transceiver circuit for the 122-GHz ISM band with antennas in package. It includes a power amplifier (PA), low-noise amplifier (LNA), quadrature mixers, a poly-phase filter, a voltage-controlled oscillator, divide-by-32 outputs and transmit and receive antennas (see Figure 1). The RF signal from the oscillator is directed to both, the TX path via PA, and to the RX path via buffer circuits. The RX signal is amplified by the LNA and converted to baseband by two mixers with quadrature LO signal. The 120-GHz VCO has four analog tuning inputs with different tuning ranges and tuning slopes. The tuning inputs can be combined to obtain a wide frequency tuning range. The analog tuning inputs together with integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With fixed oscillator frequency it can be used in continuous wave (CW) mode. Other modulation schemes are possible as well by utilizing analog tuning inputs. The IC is fabricated in a SiGe BiCMOS technology.

1.2 Applications

The main field of application for the 120-GHz transceiver radar frontend is in short range radar systems with a range up to about 10 meters. By using dielectric lenses or reflectors, the range can be increased considerably. The RFE can be used in FMCW mode as well as in CW mode. Although the chip is intended for use in the ISM band 122 GHz - 123 GHz, it is also possible to extend the bandwidth to the full tuning range of 6 GHz.

2 Block Diagram

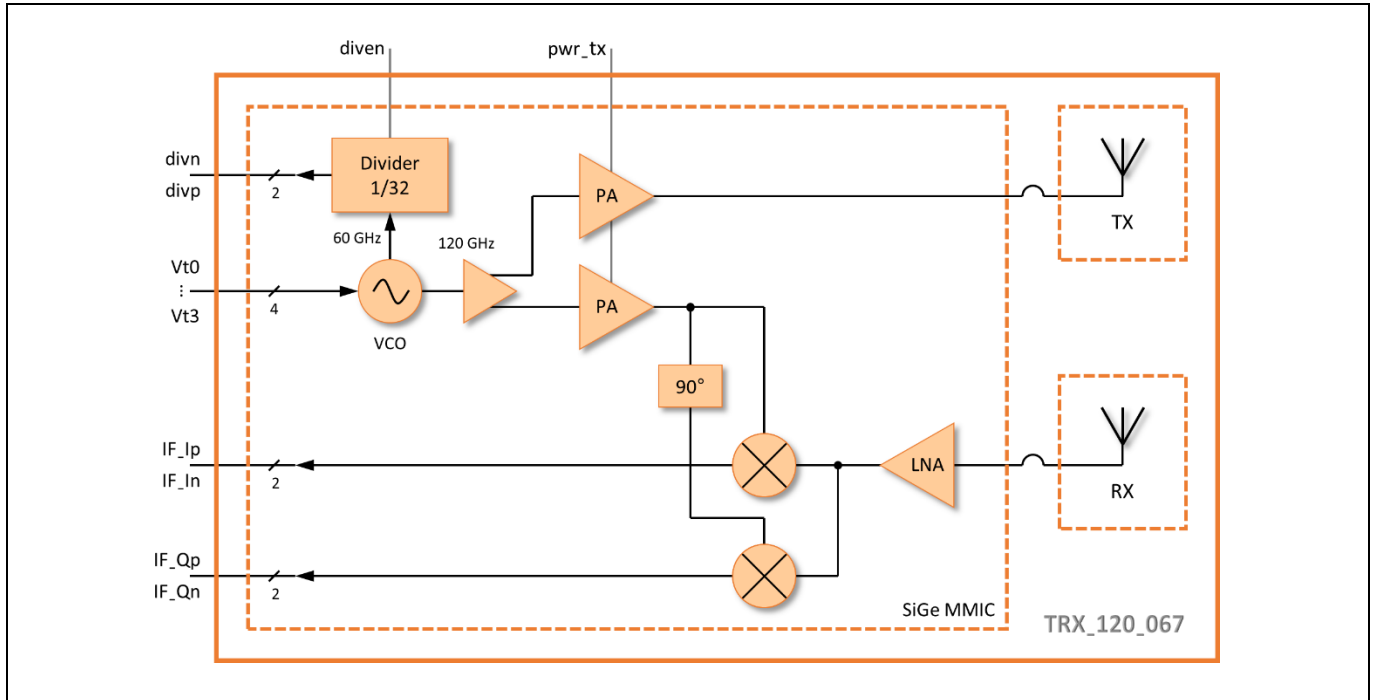


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

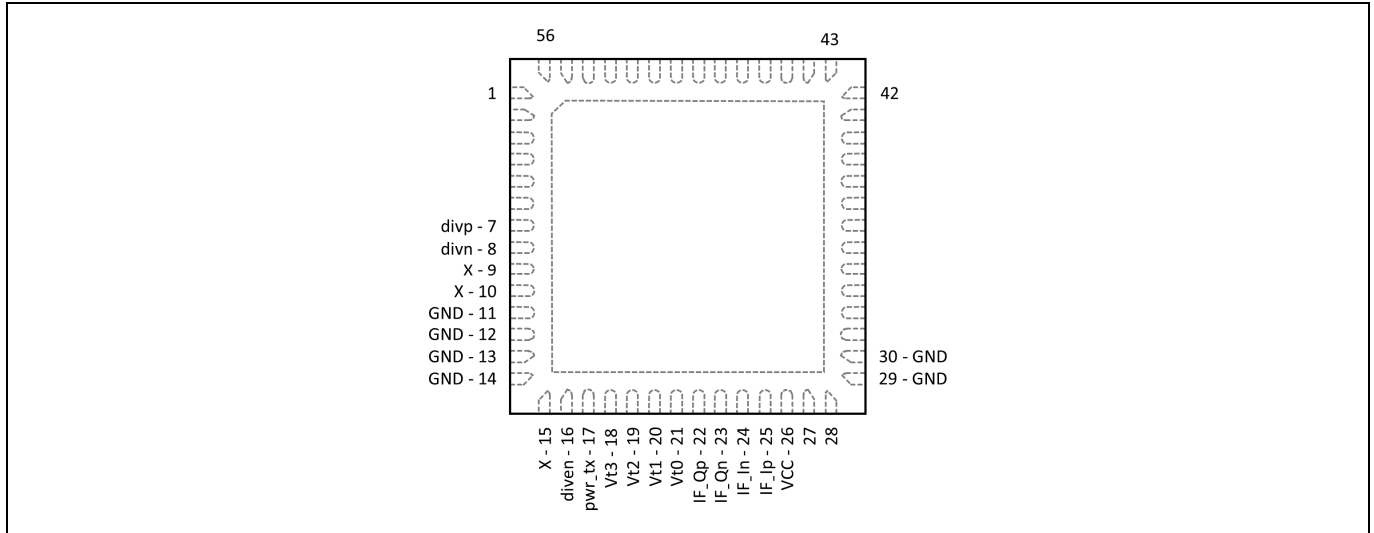


Figure 2 Pin Assignment (QFN56, top view)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
1 - 6	NC	Not connected
7	divp	Divider output with terminals for differential signal, matched to 50 Ω load, DC coupled, external decoupling capacitor required.
8	divn	
9, 10	X	Reserved. Do not make any connections.
11 - 14	GND	Connect to ground.
15	X	Reserved. Do not make any connections.
16	diven	Divider enable input: 1.2 V – enable, 0 – off. NMOS input, external pull-up resistor of 100 kΩ recommended.
17	pwr_tx	Transmitter power control input: 1.2 V – full, 0 – -3 dB. NMOS input, external pull-up resistor of 100 kΩ recommended.
18	Vt3	VCO tuning input 3 (0 – V _{CC})
19	Vt2	VCO tuning input 2 (0 – V _{CC})
20	Vt1	VCO tuning input 1 (0 – V _{CC})
21	Vt0	VCO tuning input 0 (0 – V _{CC})
22	IF_Qp	IF Q output with terminals for differential signal (DC coupled)
23	IF_Qn	
24	IF_In	IF I output with terminals for differential signal (DC coupled)
25	IF_Ip	
26	VCC	Supply voltage (3.3 V, 112 mA typ.)
27, 28	NC	Not connected
29, 30	GND	Ground pins, also connected to the exposed die attach pad.
31 - 56	NC	Not connected
(57)	GND	Exposed die attach pad of the QFN package, must be soldered to ground.

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Supply voltage	V _{CC}		3.6	V	to GND
DC voltage at tuning inputs	V _{Vt}	-0.3	V _{CC} + 0.3	V	Inputs Vt0, Vt1, Vt2, Vt3
DC voltage at enable inputs	V _{EN}	-0.3	1.5	V	Inputs diven, pwr_tx
Junction temperature	T _J	-50	150	°C	
Storage temperature range	T _{STG}		150	°C	
Floor life (out of bag) at factory ambient (30°C/60% RH)	FL		168	h	IPC/JEDEC J–STD-033A MSL Level 3 Compliant ¹⁾
ESD robustness	V _{ESD}		500	V	Human body model, HBM ²⁾

- 1) Device storage outside of the packaging is limited according to latest revision of JEDEC Standard IPC/JEDEC J–STD-033.
- 2) CLASS 1A according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Ambient temperature	T _A	-40	85	°C	
Supply voltage	V _{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning inputs	V _{Vt}	0	V _{CC}	V	Inputs Vt0 – Vt3
DC voltage at enable inputs	V _{EN}	0	1.2	V	Inputs diven, pwr_tx

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
Thermal resistance, junction-to-ambient	R _{thja}			30	K/W	JEDEC JESD51-5

4.4 Electrical Characteristics

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless otherwise noted. Typical values measured at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 3.3\text{ V}$.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
DC Parameters						
Supply current consumption	I_{CC}	100	112	128	mA	TX on, CW mode
Enable input voltage, low level	V_{EN_L}	0		0.3	V	Inputs diven, pwr_tx
Enable input voltage, high level	V_{EN_H}	0.9		1.2	V	Inputs diven, pwr_tx
VCO tuning voltage	V_{Vt}	0		V_{CC}	V	Inputs Vt0 – Vt3
RF Parameters						
VCO start frequency	f_{TX_start}	116.2	119.3	120.8	GHz	all Vt_0,1,2,3 = 0, Note 3
VCO stop frequency	f_{TX_stop}	123.3	125.4	128.9	GHz	all Vt_0,1,2,3 = 3.3 V, Note 3
VCO tuning full bandwidth	Δf_{TX}	5.5	6.3	8.2	GHz	Vt0 – Vt3 interconnected
Number of adjustable frequency bands	N	8				Vt1 – Vt3 used for band switching
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		27		MHz/V	
Phase noise	P_N		-90	-88	dBc/Hz	at 1 MHz offset
Transmitter output power	P_{TX}	-7	-3	1	dBm	Measured without antennas, $V(pwr_tx) = 1.2\text{ V}$
EIRP RMS Power	$P_{TX_EIRP_RMS}$		7.7		dBm	Measured at $T_A = 25^{\circ}\text{C}$, FMCW, Duty Cycle 100%, Note 2
Divider ratio of TX signal	N_{div}	64				
Divider output power	P_{div}	-10		-7	dBm	Note 1
Divider output frequency	f_{div}	1.84		1.99	GHz	
Receiver gain	g_{RX}		8	10	dB	Measured without antennas
IF frequency range	f_{IF}	0		200	MHz	
IF output impedance	Z_{OUT}		500		Ω	Differential outputs
IQ amplitude imbalance	Aimb	-1.5		+1.5	dB	
IQ phase imbalance	PHimb	-10		10	deg	
Noise figure (DSB)	NF		8.7		dB	Simulated, at $f_{IF} = 1\text{ MHz}$
Input compression point	1dB ICP		-20		dBm	Measured without antennas

Note 1: Measured single-ended. Divider outputs are loaded with $50\ \Omega$, external decoupling capacitors are required. $50\text{-}\Omega$ match is not required in application.

Note 2: FMCW band width = 1.0 GHz

Note 3: Operation within world-wide ISM Band and over the entire ambient temperature range. Further information available.

5 Packaging

5.1 Outline Dimensions

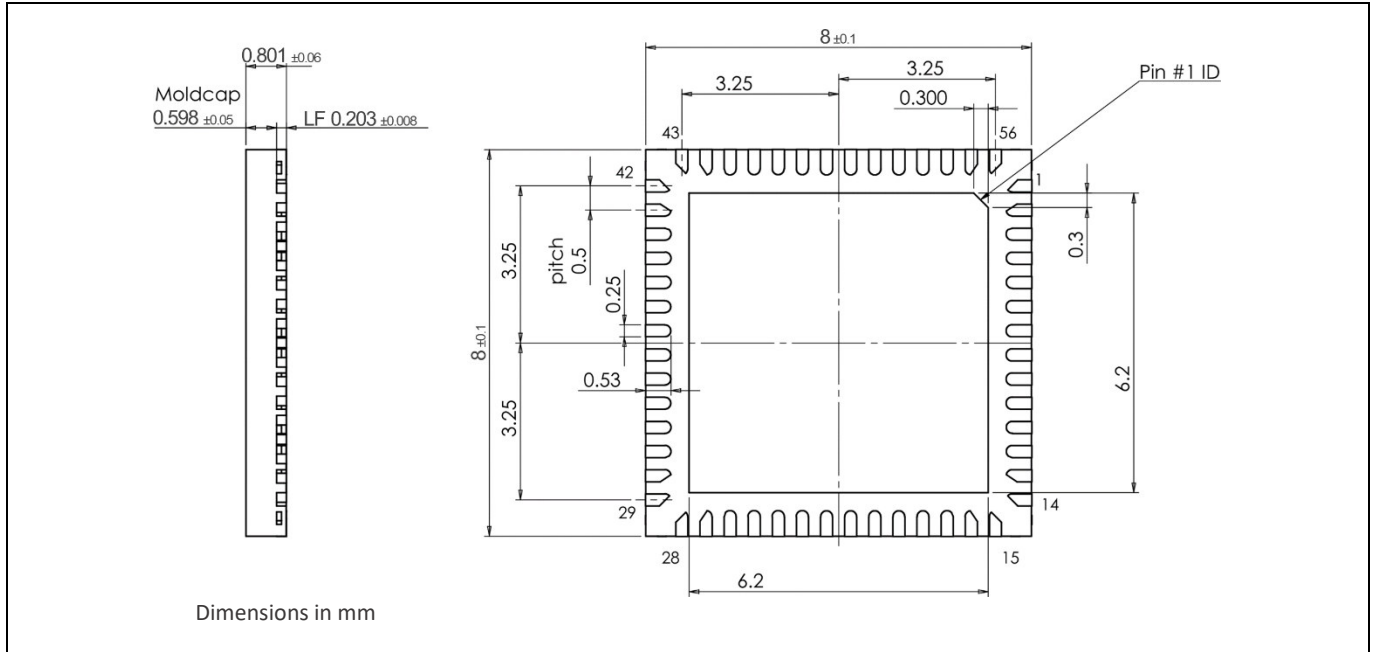


Figure 3 Outline Dimensions of QFN56, 0.5 mm Pitch, 8 mm × 8 mm

5.2 Package Code

Top-Side Markings

TRX067
 YYWW

5.3 Antenna Position

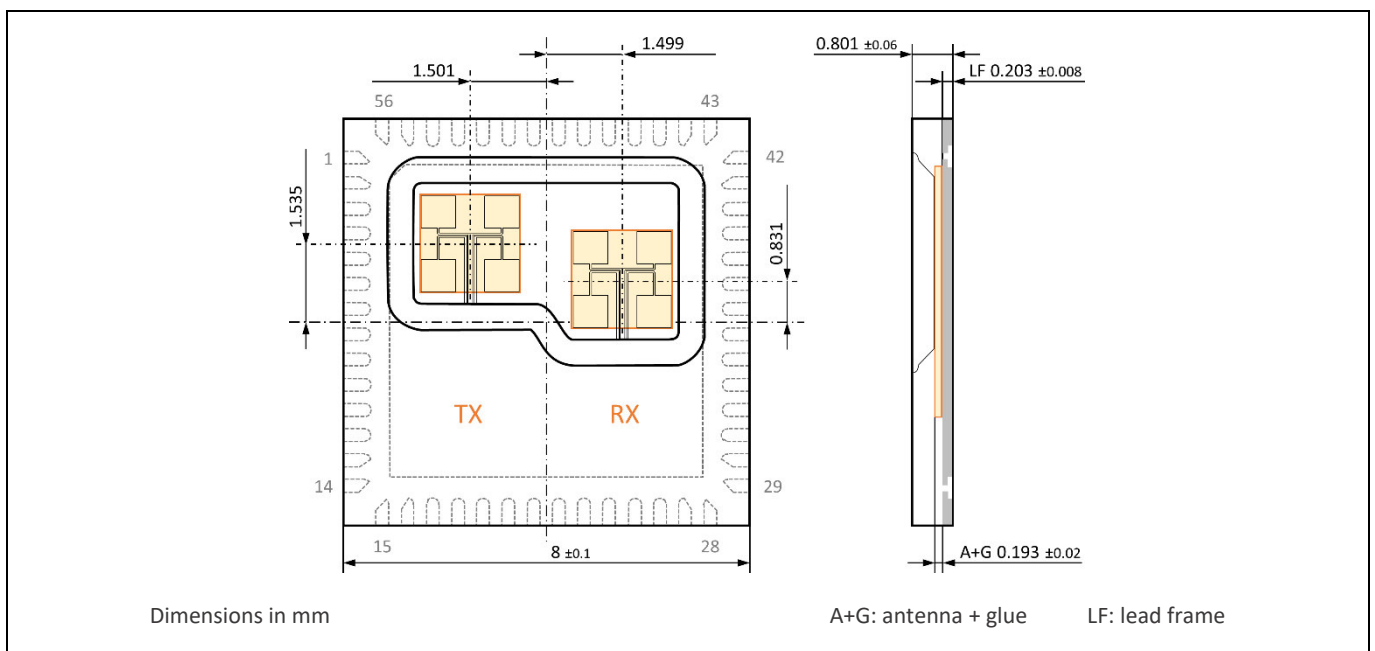


Figure 4 Position of Antenna Arrays (top view) and Cross Section (through RX Antenna)

6 Application

6.1 Application Circuit Schematic

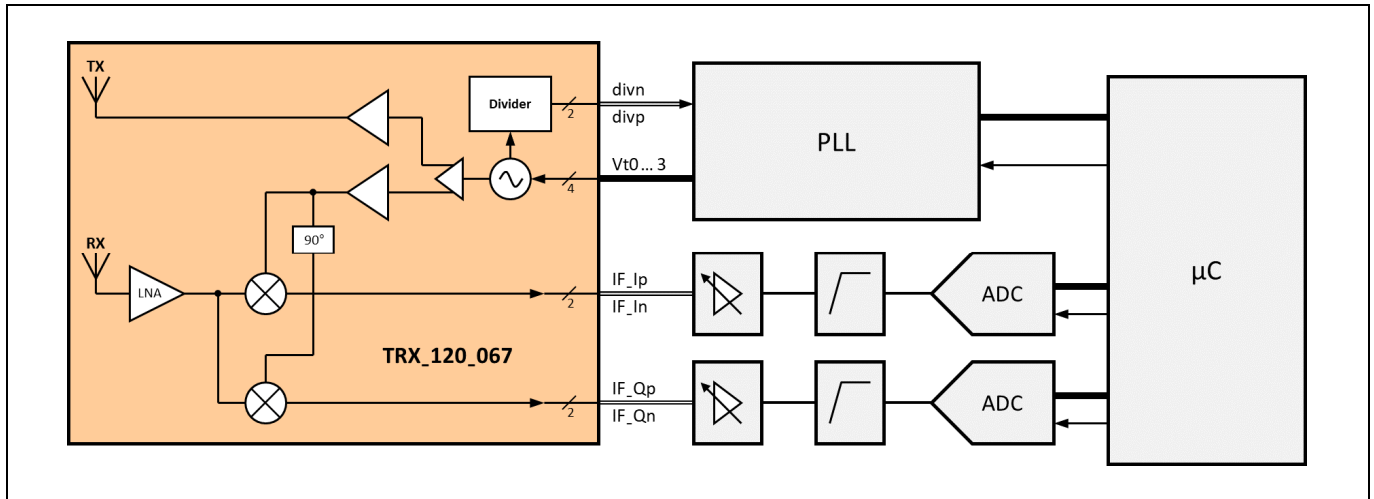


Figure 5 Application Circuit

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 μ s and 100 μ s is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Kit

Silicon Radar offers evaluation kits for speeding up radar development. Please review our website and product sheets for more information: <https://www.siliconradar.com/evalkits/>.

The *SiRad Easy[®] r4* platform supports development for many of Silicon Radar's integrated IQ transceivers including radar front end boards for TRX_120_067. It serves as reference hardware and provides a design environment including a graphical user interface for parameter setting. Its functionality and communication protocol are adaptable to development projects.

6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

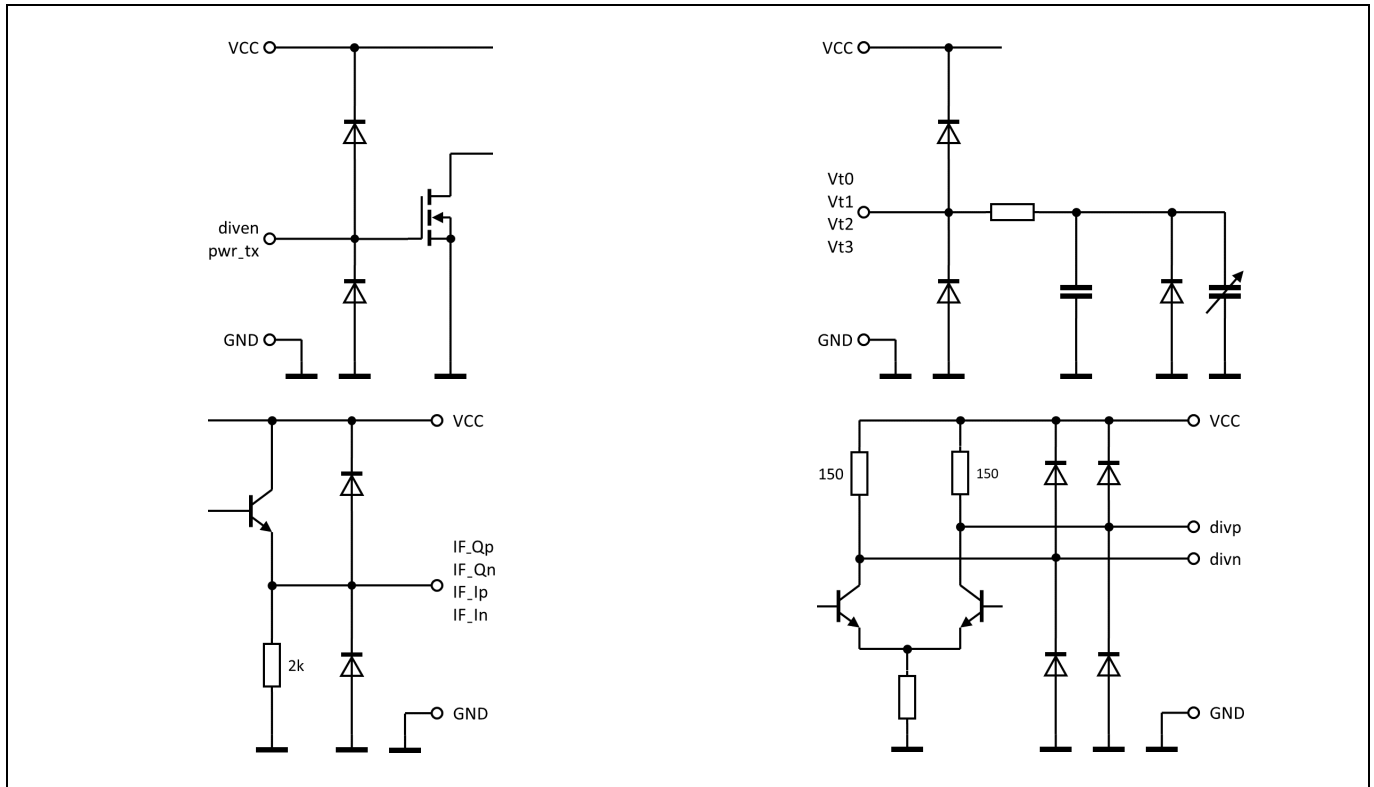


Figure 6 Equivalent I/O Circuits

6.5 VCO Tuning Inputs

The VCO tuning inputs V_{t0} – V_{t3} are of analog nature but can be switched digitally as well. The tuning inputs differ in their tuning ranges (tuning bandwidth) and slopes, whereby V_{t3} has the widest tuning range, and V_{t0} the narrowest.

Table 6 Typical VCO Tuning Bandwidth and Slope

Input	VCO tuning bandwidth (MHz)		Middle band slope (MHz/V)	
V_{t0}	$\Delta f_{TX,V_{t0}}$	720	$\Delta f_{TX} / \Delta V_{V_{t0}}$	290
V_{t1}	$\Delta f_{TX,V_{t1}}$	750	$\Delta f_{TX} / \Delta V_{V_{t1}}$	300
V_{t2}	$\Delta f_{TX,V_{t2}}$	1580	$\Delta f_{TX} / \Delta V_{V_{t2}}$	630
V_{t3}	$\Delta f_{TX,V_{t3}}$	3450	$\Delta f_{TX} / \Delta V_{V_{t3}}$	1380

The VCO tuning range of a specific tuning input can be increased by connecting it to another tuning input. All combinations of the four tuning inputs are allowed. Unused tuning inputs must be set to a fixed potential (between 0 and V_{CC}). The interconnection of all inputs V_{t0} – V_{t3} leads to the maximum tuning bandwidth. For example, if V_{t0} is used as tuning input, the variation of the potential at V_{t1} , V_{t2} , V_{t3} in all logical combinations of 0 and V_{CC} , results in offsetting the tuning curve (see Figure 10).

7 Reliability and Environmental Test

Table 7 Reliability and Environmental Test according to JEDEC Standards

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	pass
Temperature Cycling	JESD22-A104	850 cycles at -40°C ... 125°C	pass
HTSL	JESD22-A103	1,000 h at 150°C	pass
HTOL	JESD22-A108	1,000 h at 85°C	pass
THB	JESD22-A101	1,000 h at 85°C and 85% RH	pass

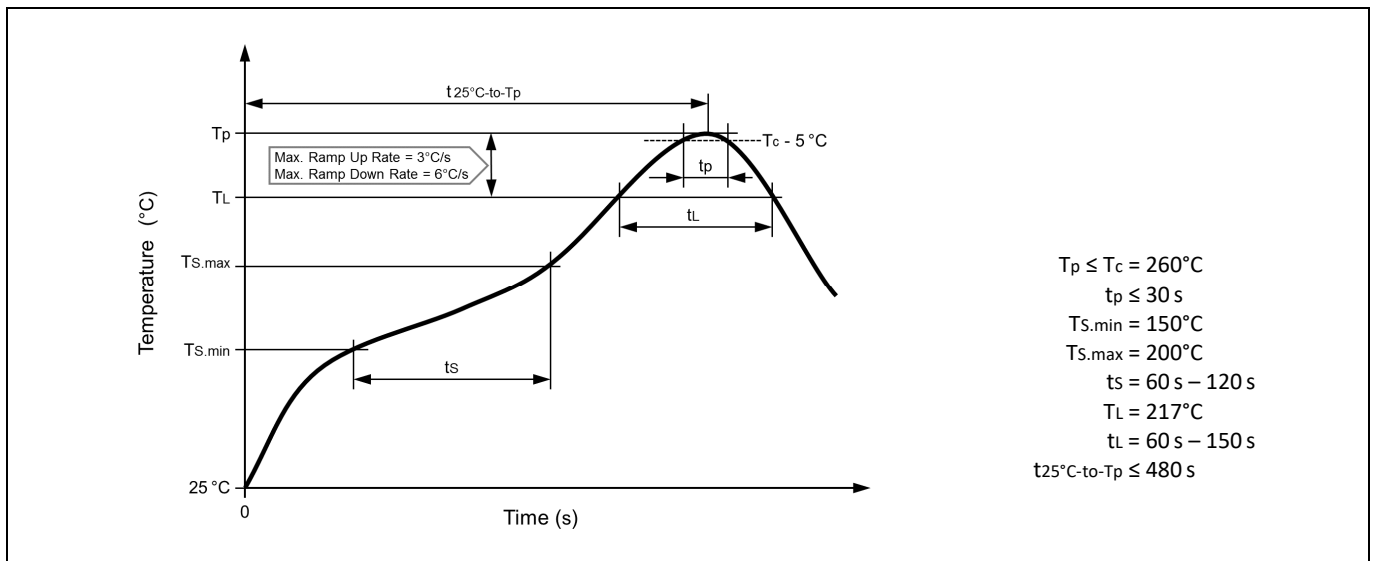


Figure 7 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

8 Measurement Results

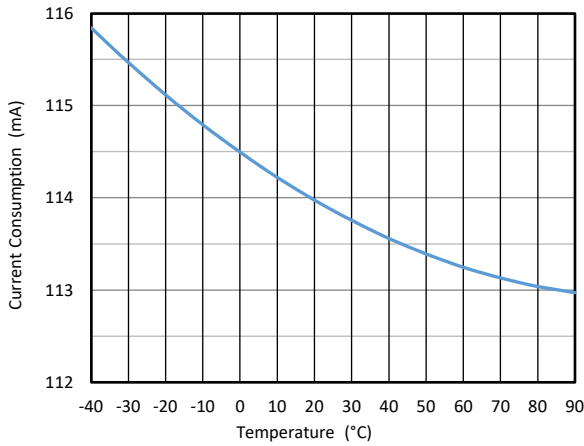


Figure 8 Current Consumption vs. Temperature

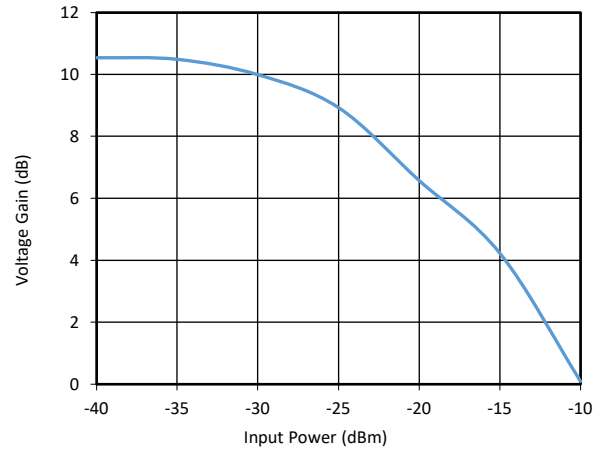


Figure 9 Measured Conversion Gain of the Receiver without antenna

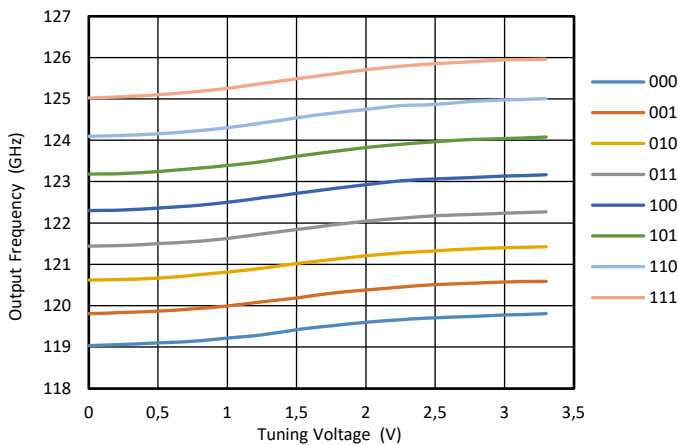


Figure 10 VCO Tuning Curves. V_{t0} is varied, while V_{t1} , V_{t2} and V_{t3} are driven high or low. For example, 011 means $V_{t3} = 0$, $V_{t2} = 3.3\text{ V}$, and $V_{t1} = 3.3\text{ V}$.

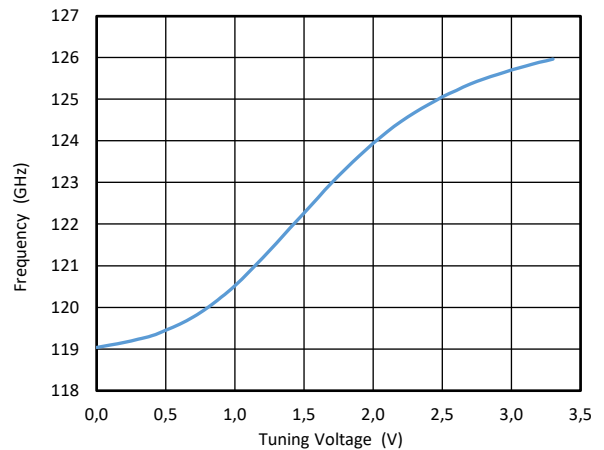


Figure 11 Full Bandwidth VCO Tuning. V_{t0} , V_{t1} , V_{t2} , V_{t3} are interconnected. ($V_{t0} = V_{t1} = V_{t2} = V_{t3}$)

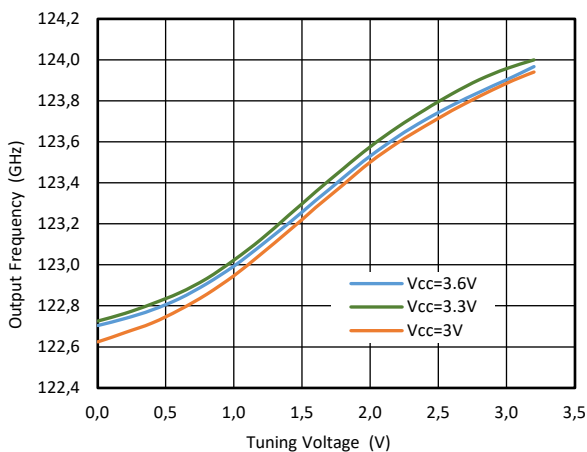


Figure 12 VCO Pushing - $V_{cc} \pm 300\text{ mV}$
 $V_{t0} = \text{sweep}$, $V_{t1} = V_{t2} = 0$, $V_{t3} = 3.3\text{ V}$

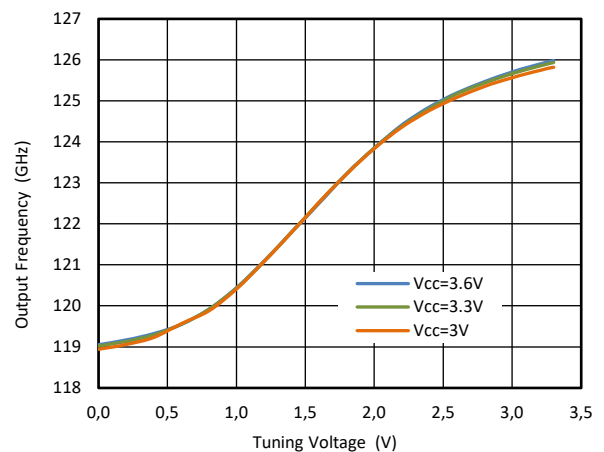


Figure 13 VCO Pushing - Full Bandwidth Operation. All tuning voltages, $V_{t0} = V_{t1} = V_{t2} = V_{t3}$

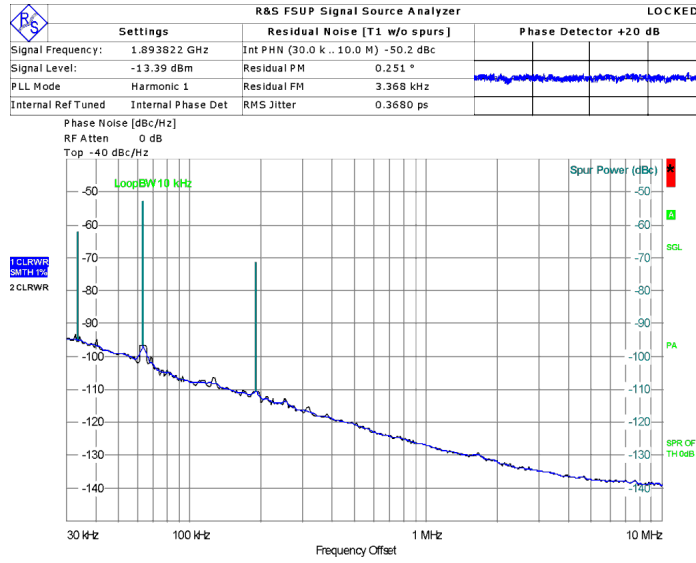


Figure 14 Phase Noise of the Integrated Oscillator Measured at Divider Output (1.89 GHz)

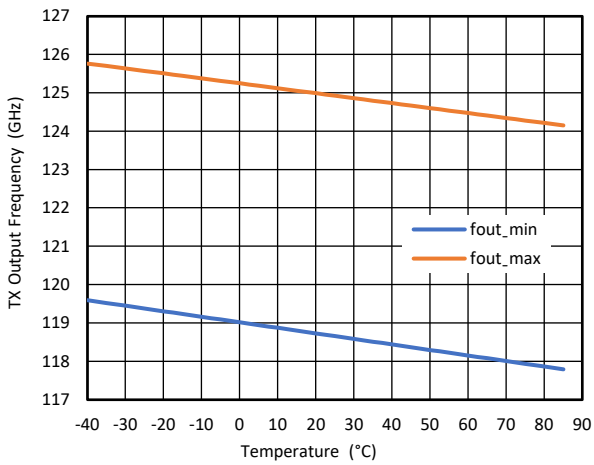


Figure 15 TX Output Frequency vs. Temperature

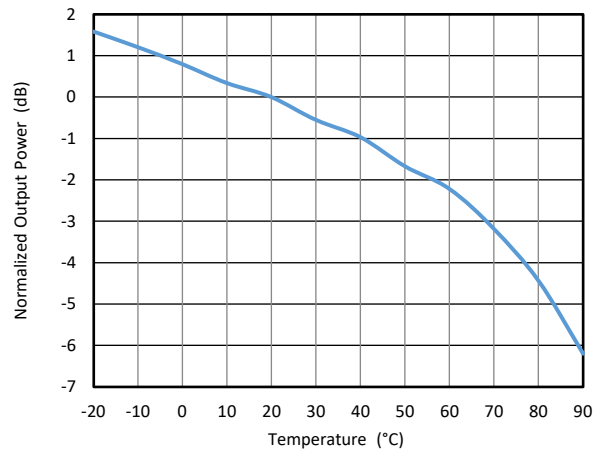


Figure 16 TX Output Power vs. Temperature (Normalized to 20°C)

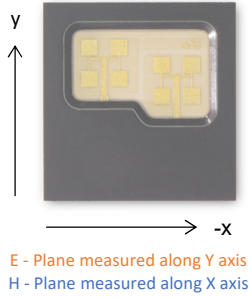


Figure 17 MMIC Orientation for Antenna Measurements

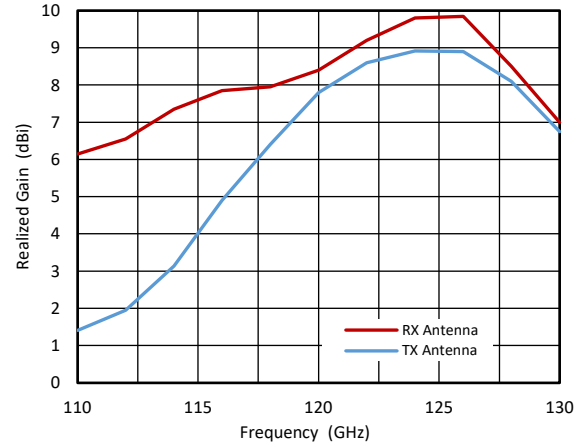


Figure 18 Simulated Single Antenna Gain vs. Frequency (Broad Side Direction)

The result of the measurements of the radiation patterns of TX and RX patch antennas at different frequencies are shown in Figure 19. The power levels are normalized separately for RX and TX measurements.

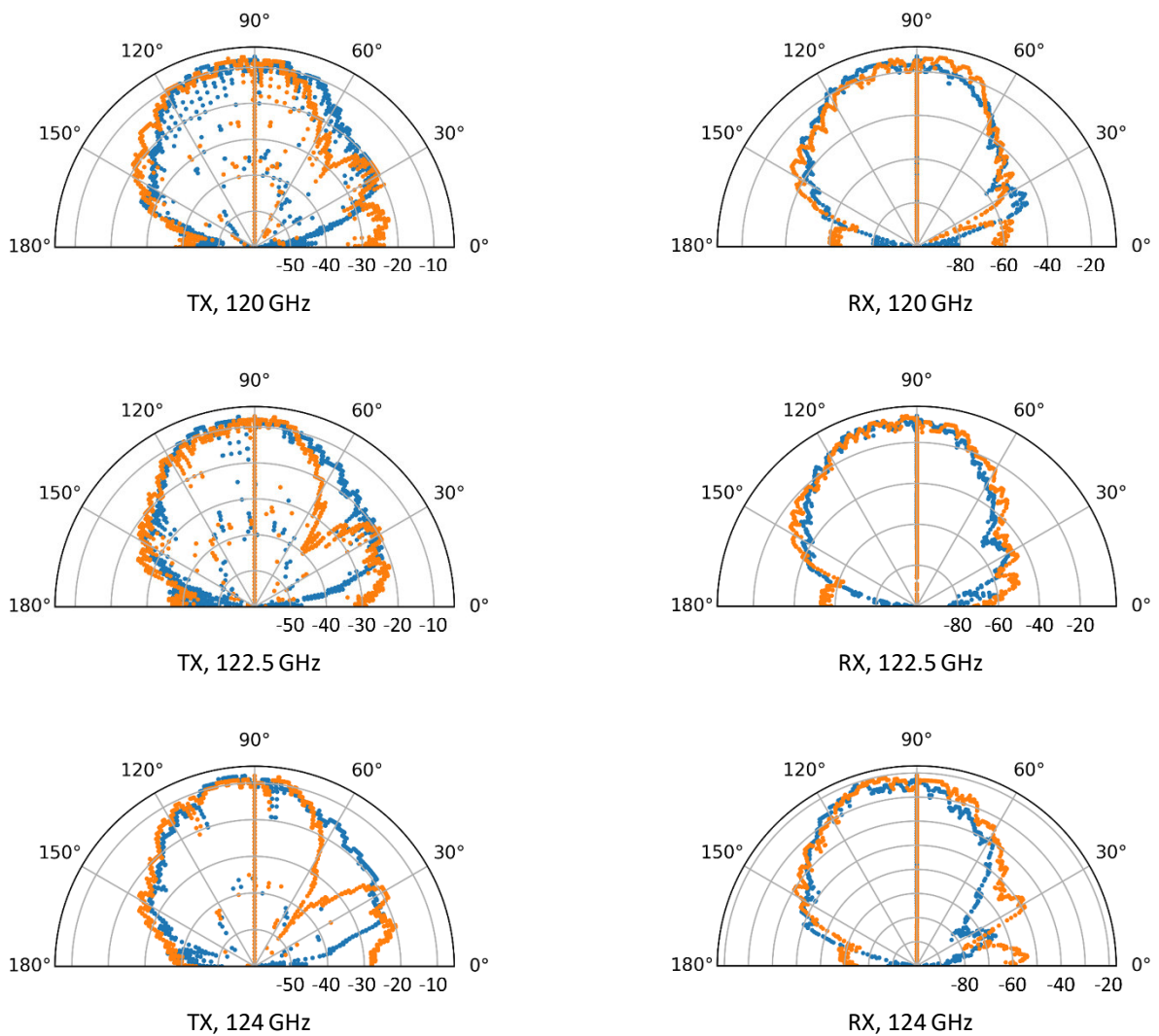


Figure 19 Radiation Pattern of TX and RX Patch Antennas, measured at different frequencies – H-Plane (blue), E-Plane (orange)

The combined normalized radiation patterns of RX and TX antenna for FMCW operation are shown in Figure 20. During the measurement, the IC was operated in FMCW mode with a bandwidth of 1 GHz. A corner reflector was used as the target. The frequency of the measurement refers to the start frequency of the sweep.

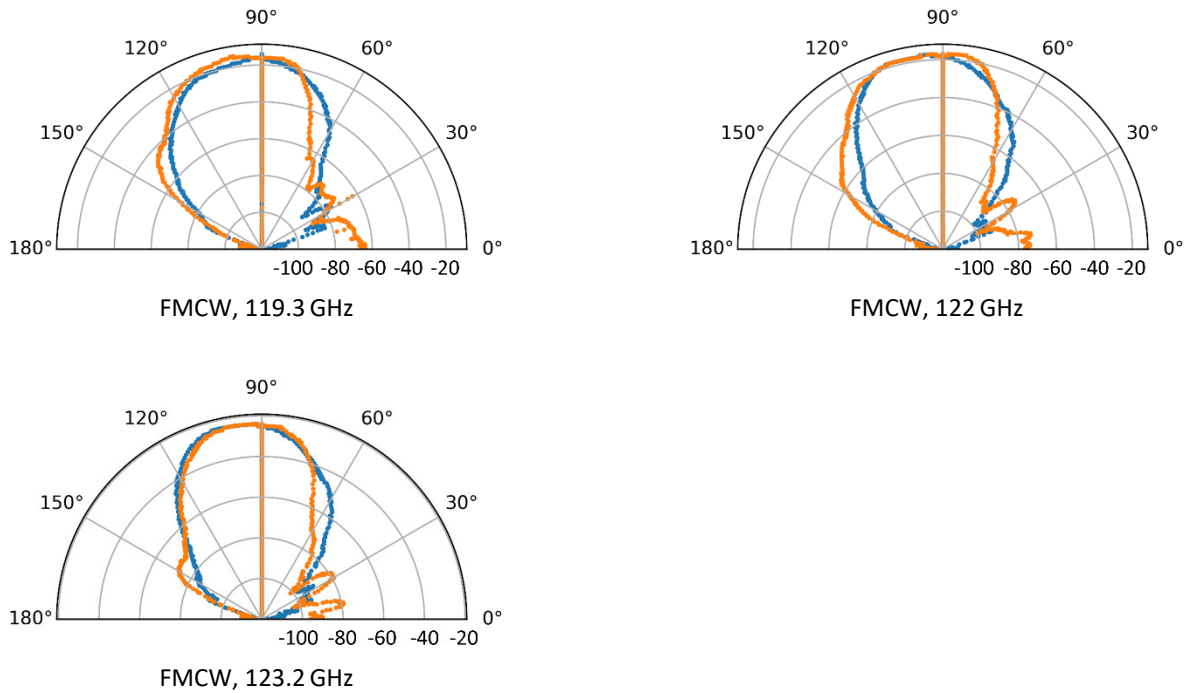


Figure 20 Combined Radiation Pattern of TX and RX Patch Antennas, measured in FMCW mode with 1-GHz modulation bandwidth at different frequencies – H-Plane (blue), E-Plane (orange)

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