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TR2_120_017

120-GHz Highly Integrated IQ Transceiver with Antennas in Package
in Silicon Germanium Technology

Preliminary Data Sheet

Status:	Date:	Author:	Filename:	
Preliminary	08-Sep-2023	Indie Semiconductor FFO GmbH	Datasheet_TR2_120_017	
Version: 0.4	Product number: TR2_120_017	Package: LGA66, 6 × 10 mm²	Marking: T2R17 YYWW	Page: 1 of 16
Document:	Annex to VA_U03_01	Anlage 8_Template_Datenblatt_RevE	Date: 19-May-2020	Rev E

Version Control

Version	Changed section	Description of change	Reason for change
0.1	(all)	Creation of initial version of document	
0.2	3.2 6.3 7	Updated pin names Updated I/O circuits Updated Figure 11 and Figure 13	To make consistent with TRX_120_001 Latest results were taken
0.3	3.2 3.3	Changed the sub-section name from “Pin Description” to “Netlist Package” Added	To illustrate the pin names in the form of matrix for the package Copied the contents of previously sub-section 3.2 into 3.3
0.4	5.1	Updated	Inserted drawings from packaging supplier

Table of Contents

1 Features

- Radar front end (RFE) with antennas in package for 122-GHz ISM band
- One transmit and two receive channels
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 760 mW in continuous operating mode
- Duty Cycling possible
- Integrated low phase noise push-push VCO
- Receiver with homodyne quadrature mixer
- Wide bandwidth of up to 7.5 GHz
- LGA66 leadless package 6 × 10mm²
- Pb-free, RoHS compliant package

1.1 Overview

The TR2_120_017 is an integrated transceiver circuit for the 122 – 123 GHz ISM band with antennas in package consisting of one transmit and two receive channels (see Figure 1). The transmitter channel features a gain-controlled power amplifier (PA) and each of the two receiver channels has a gain-controlled low-noise amplifier (LNA), a quadrature mixer and poly-phase filter. The transceiver features a 120 GHz voltage-controlled oscillator (VCO) with a differential divider output. The analog inputs - Vfine and Vcoarse, tune the VCO frequency. The RF signal from the oscillator is directed to the RX and TX paths via a local oscillator (LO) amplifier followed by a 3-way power divider. In each channel, the RX signal is amplified by the LNA and converted to baseband by the quadrature mixer. The analog tuning inputs together with the integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With fixed oscillator frequency it can be used in continuous wave (CW) mode. Other modulation schemes are possible as well by utilizing analog tuning inputs. The IC has been fabricated in SiGe BiCMOS technology.

1.2 Applications

The main field of application for the 120 GHz transceiver radar frontend is in short range radar systems with a range up to about 10 meters. By using dielectric lenses or reflectors, the range can be increased considerably. The TR2_120_017 can be used in FMCW mode as well as in CW mode. Although the chip is intended for use in the ISM band 122 GHz - 123 GHz, it is also possible to extend the bandwidth to the full tuning range of typ. 6.7 GHz. Its high operating frequency and high output power allows measurements with improved range accuracy and maximum detection range. The two receiver channels provide a radar structure where angular resolution is increased, and target angle of arrival measurements can be performed.

2 Block Diagram

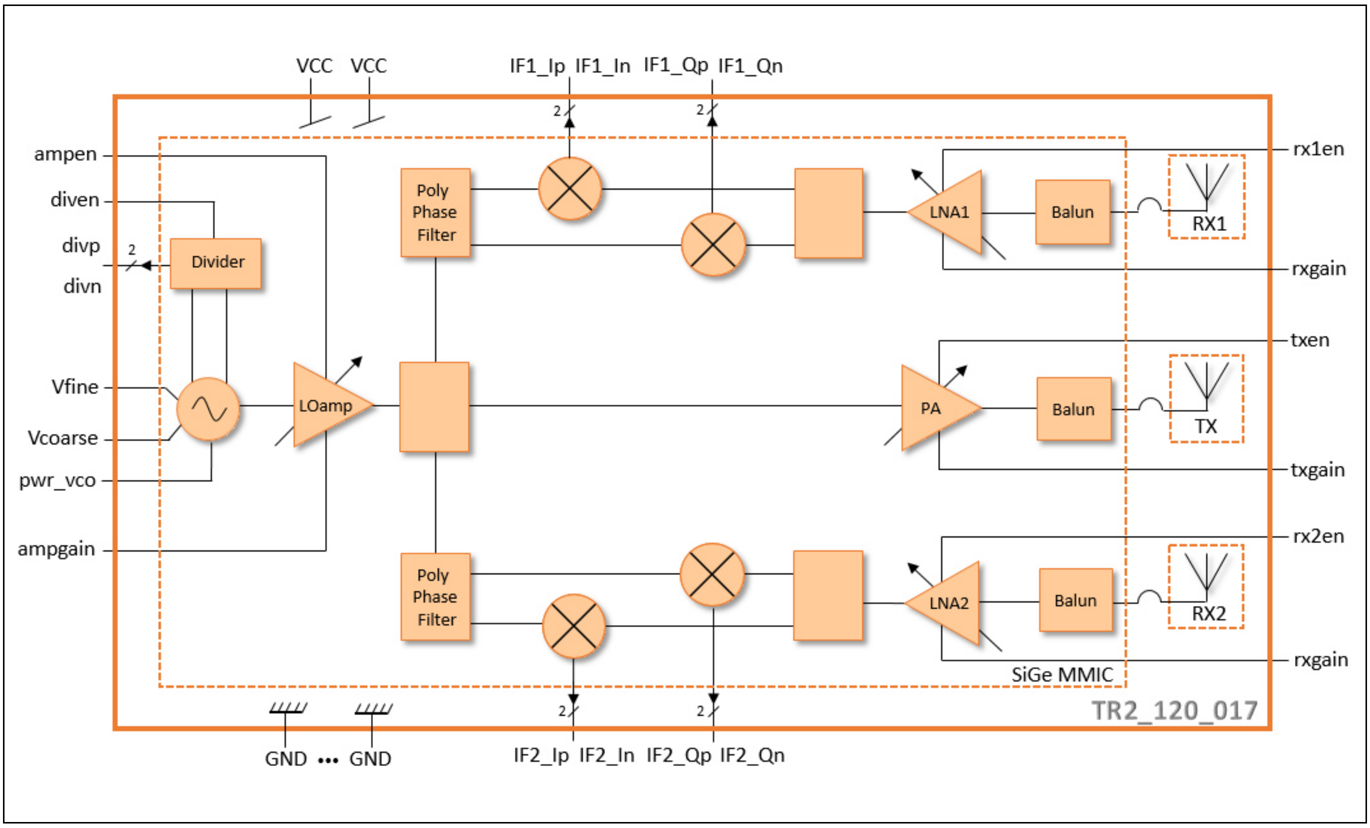


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

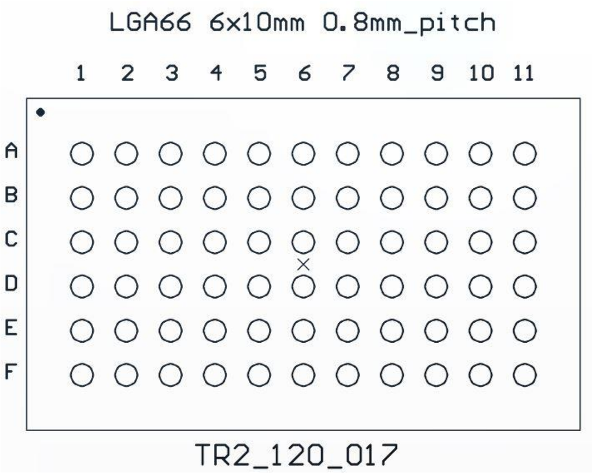


Figure 2 Pin Assignment (LGA66, top view)

3.2 Netlist Package

Table 1 Netlist Package (top view)

	1	2	3	4	5	6	7	8	9	10	11
A	GND	txen	txgain	rx2en	GND	VCC	rx1en	rxgain	IF1_In	IF1_Ip	IF1_Qn
B	GND	GND	GND	GND	GND	VCC	GND	GND	GND	GND	IF1_Qp
C	GND	GND	GND	GND	GND	VCC	GND	GND	GND	GND	GND
D	GND	GND	GND	GND	GND	VCC	GND	GND	GND	GND	GND
E	divp	GND	GND	GND	GND	VCC	GND	GND	GND	GND	IF2_Qp
F	divn	diven	pwr_vco	Vfine	Vcoarse	VCC	ampen	ampgain	IF2_In	IF2_Ip	IF2_Qn

3.3 Pin Description

Table 2 Pin Description

Pin		Description
No.	Name	
A1	GND	Ground pad
A2	txen	PA enable (input with Schmitt trigger), no pull-up / pull-down resistors. By default, PA is off : 0 V (PA disable) / 3.3 V (PA enable), ***digital***
A3	txgain	PA gain control voltage with pull-down resistor of 100 kOhm. By default, PA is set to low output power operation mode: 0 V (PA set to low output power mode) - 3.3 V (PA set to high output power mode), ***analogue***. Active gain setting voltage levels are kept between 1.3 V (lowest output power) – 2.0 V (highest output power).
A4	rx2en	RX channel 2 enable (input with Schmitt trigger), no pull-up / pull-down resistors. By default, RX channel is off: 0 V (RX channel disable) / 3.3 V (RX channel enable), ***digital***
A5	GND	Ground pad
A6	VCC	Chip supply voltage: 3.3 V
A7	rx1en	RX channel 1 enable (input with Schmitt trigger), no pull-up / pull-down resistors. By default, RX channel is off: 0 V (RX channel disable) / 3.3 V (RX channel enable), ***digital***

A8	rxgain	RX channel 1 and RX channel 2 gain control voltage (input with Schmitt trigger), no pull-up / pull-down resistors. By default, both RX channels have low gain: 0 V (RX channel low gain) / 3.3 V (RX high gain), ***digital***
A9	IF1_In	IF I output for RX1, negative terminal
A10	IF1_Ip	IF I output for RX1, positive terminal
A11	IF1_Qn	IF Q output for RX1, negative terminal
B1-B5	GND	Ground pad
B6	VCC	Chip supply voltage: 3.3 V
B7-B10	GND	Ground pad
B11	IF1_Qp	IF Q output for RX1, positive terminal
C1-C5	GND	Ground pad
C6	VCC	Chip supply voltage: 3.3 V
C7-C11	GND	Ground pad
D1-D5	GND	Ground pad
D6	VCC	Chip supply voltage: 3.3 V
D7-D11	GND	Ground pad
E1	divp	Frequency divider differential output (1.9 GHz – 2 GHz)
E2-E5	GND	Ground pad
E6	VCC	Chip supply voltage: 3.3 V
E7-E10	GND	Ground pad
E11	IF2_Qp	IF Q output for RX2, positive terminal
F1	divn	Frequency divider differential output (1.9 GHz – 2 GHz)
F2	diven	Frequency divider enable (input with Schmitt trigger), no pull-up / pull-down resistors. By default, frequency divider is off: 0 V (Frequency Divider disable) / 3.3 V (Frequency Divider enable), ***digital***
F3	pwr_vco	VCO gain control voltage (input with Schmitt trigger), no pull-up / pull-down resistors. By default, VCO is set to low gain operation mode: 0 V (VCO low gain) / 3.3 V (VCO high gain), ***digital***
F4	Vfine	VCO frequency tuning voltages: 0 V – 3.3 V (121 GHz – 128.5 GHz), ***analogue***
F5	Vcoarse	
F6	VCC	Chip supply voltage: 3.3 V
F7	ampen	LOamp enable (input with Schmitt trigger), no pull-up / pull-down resistors. By default, LOamp is off: 0 V (LOamp disable) / 3.3 V (LOamp enable), ***digital***
F8	ampgain	LOamp gain control voltage with pull-down resistor of 100 kOhm. By default, LOamp is set to low output power operation mode: 0 V (LOamp set to low output power mode) - 3.3 V (LOamp set to high output power mode), ***analogue***. Active gain setting voltage levels are kept between 1.3 V (lowest output power) – 2.0 V (highest output power).
F9	IF2_In	IF I output for RX2, negative terminal
F10	IF2_Ip	IF I output for RX2, positive terminal
F11	IF2_Qn	IF Q output for RX2, negative terminal

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Supply voltage	V_{CC}		3.6	V	to GND
DC voltage at RF pins	V_{DCRF}	0	2	mV	Low ohmic connection to GND: TX, RX1 and RX2 pins; DC coupled: div outputs and IF pins
DC voltage at tuning inputs	V_{Vt}	-0.17	V_{CC} +0.17	V	Inputs: Vfine, Vcoarse
DC voltage at enable inputs	V_{EN}	-0.17	V_{CC} +0.17	V	Inputs: ampen, diven, txen, rx1en, rx2en
DC voltage at gain control pins	V_{CTRL}	-0.17	V_{CC} +0.17	V	ampgain, txgain, rxgain, pwr_vco
Junction temperature	T_J	-50	150	°C	
Storage temperature range	T_{STG}		150	°C	
ESD robustness	V_{ESD}		tbd	V	

4.2 Operating Range

Table 4 Operating Range

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning inputs	V_{Vt}	0	V_{CC}	V	Inputs: Vfine, Vcoarse
DC voltage at enable inputs	V_{EN}	0	V_{CC}	V	Inputs: diven, txen, rx1en, rx2en

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 5 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
Thermal resistance, junction-to-ambient	R_{thja}			30	K/W	JEDEC JESD51-5

4.4 Electrical Characteristics

T_A = -40°C to +85°C unless otherwise noted. Typical values measured at T_A = 25°C and V_{CC} = 3.3 V.

Table 6 Electrical Characteristics

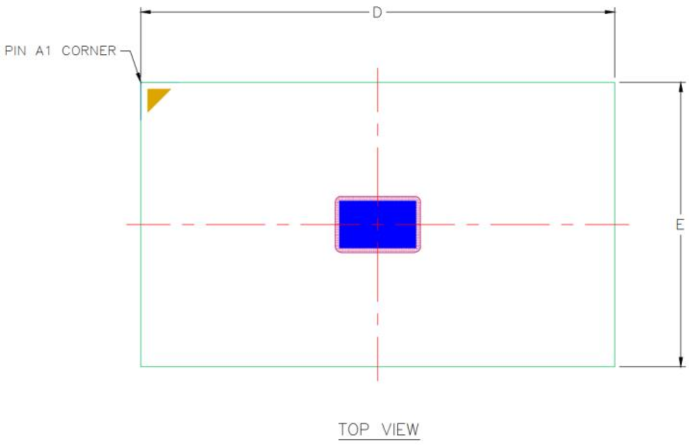
Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
DC Parameters						
Supply current consumption	I_{CC}	220	230	245	mA	Enabled all, max gain
Enable input voltage, low level	V_{EN_L}	0	0	0.3	V	Inputs: ampen, diven, txen, rx1en, rx2en
Enable input voltage, high level	V_{EN_H}	V_{CC} - 0.17	V_{CC}	V_{CC} + 0.17	V	Inputs: ampen, diven, txen, rx1en, rx2en
VCO tuning voltage	V_{Vt}	0		V_{CC}	V	Inputs: Vfine, Vcoarse
RF Parameters						
VCO start frequency	f_{TX}	116.1	*tbd*	121.7	GHz	Vfine = Vcoarse = 0
VCO stop frequency	f_{TX}	123.3	*tbd*	128.9	GHz	Vfine = Vcoarse = 3.3 V
VCO tuning full bandwidth	Δf_{TX}	*tbd*	6.5	*tbd*	GHz	
Number of adjustable frequency bands			2			
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		374		MHz/V	
Phase noise	P_N		-90		dBc/Hz	at 1 MHz offset
Transmitter output power	P_{TX}		3.0		dBm	Measured without antennas
Divider ratio of TX signal	N_{div}		64			
Divider output power	P_{div}	> -20	tbd		dBm	Vfine = Vcoarse = 3.3 V, Note 1
Divider output frequency	f_{div}		1.9		GHz	f_{TX}/64
Receiver conversion gain	g_{RX}	> 10	tbd		dB	Voltage conversion gain
IF frequency range	f_{IF}	0		200	MHz	
IF output impedance	Z_{OUT}		500		Ω	Differential outputs
IQ amplitude imbalance			< +/-1.5		dB	Voltage gain difference measured at f_{IF} = 5 MHz
IQ phase imbalance		-10		10	deg	
Noise figure (DSB)			12.5		dB	Simulated, at f_{IF} = 1 MHz
Input compression point	IP1dB		-20		dBm	

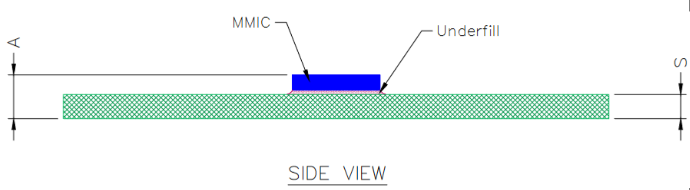
Note 1: Divider outputs are loaded with 50 Ω, external decoupling capacitors are required. No 50-Ω match is required in application.

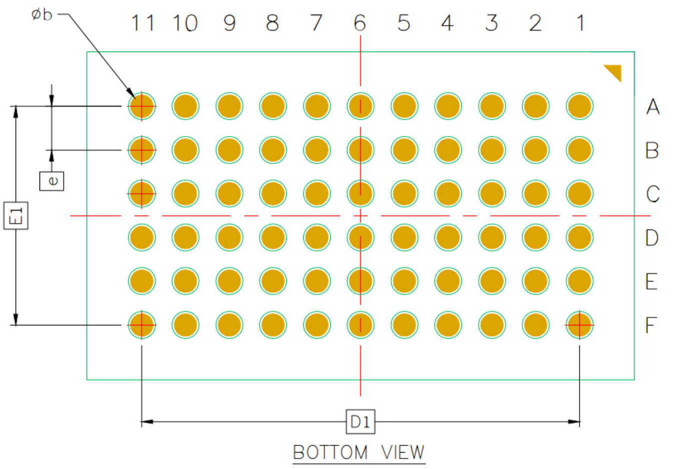
5 Packaging

5.1 Outline Dimensions

w/o Mold & Solder %alls







SYMBOL	Package Dimension					
	Millimeters			Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.	0.6	0. 7	0.02	0.026	0.0
b	0.39	0.40	0.41	0.015	0.016	0.0161
D	9.95	10.00	10.05	0.392	0.394	0.396
D1	8.00 BSC			0.315 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	4.00 BSC			0.157 BSC		
e	0.80 BSC			0.031 BSC		
S	0.416	0.446	0.476	0.016	0.018	0.019

NOTES:

- ALL DIMENSIONS IN MILLIMETERS
- PACKAGE IS SAW SINGULATED
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M
- UNDERFILL < 1.0mm FROM DIE PERIMETER.
- DIE CENTER LOCATION IS AT THE CENTER OF THE DEVICE WITH AN ACCURACY OF 30 um

Figure 3 Outline Dimensions of LGA66, 0.8 mm Pitch, 6 mm × 10 mm

5.2 Package Code

Top-Side Markings: T2R17
YYWW

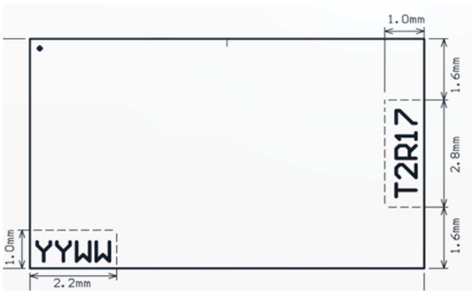


Figure 4 Package Marking

5.3 Antenna Position

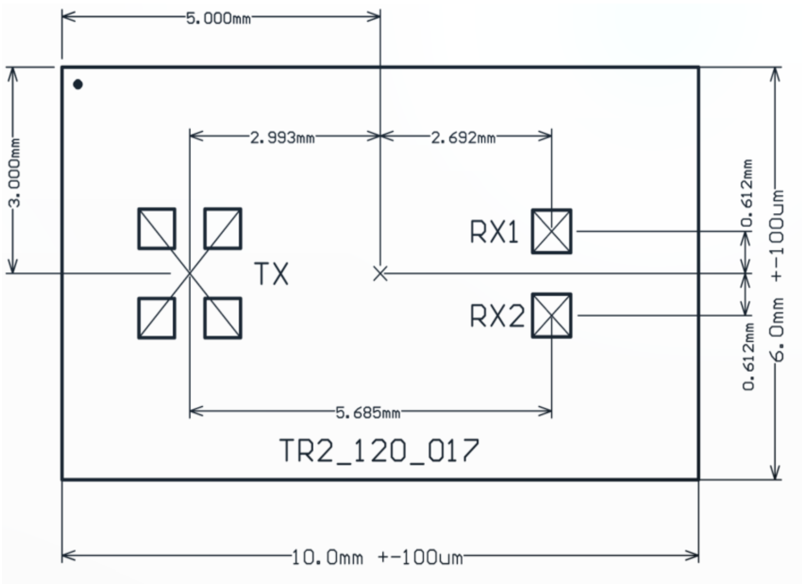


Figure 5 Antenna Position (top view)

6 Application

6.1 Evaluation Kit

Silicon Radar offers evaluation kits for speeding up radar development. Please review our website and product sheets for more information: https://www.siliconradar.com/evalkits/.
The *SiRad Easy® r4* platform supports development for many of Silicon Radar's integrated IQ transceivers including radar front end boards for TR2_120_017. It serves as reference hardware and provides a design environment including a graphical user interface for parameter setting. Its functionality and communication protocol are adaptable to development projects.

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and 100 µs is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

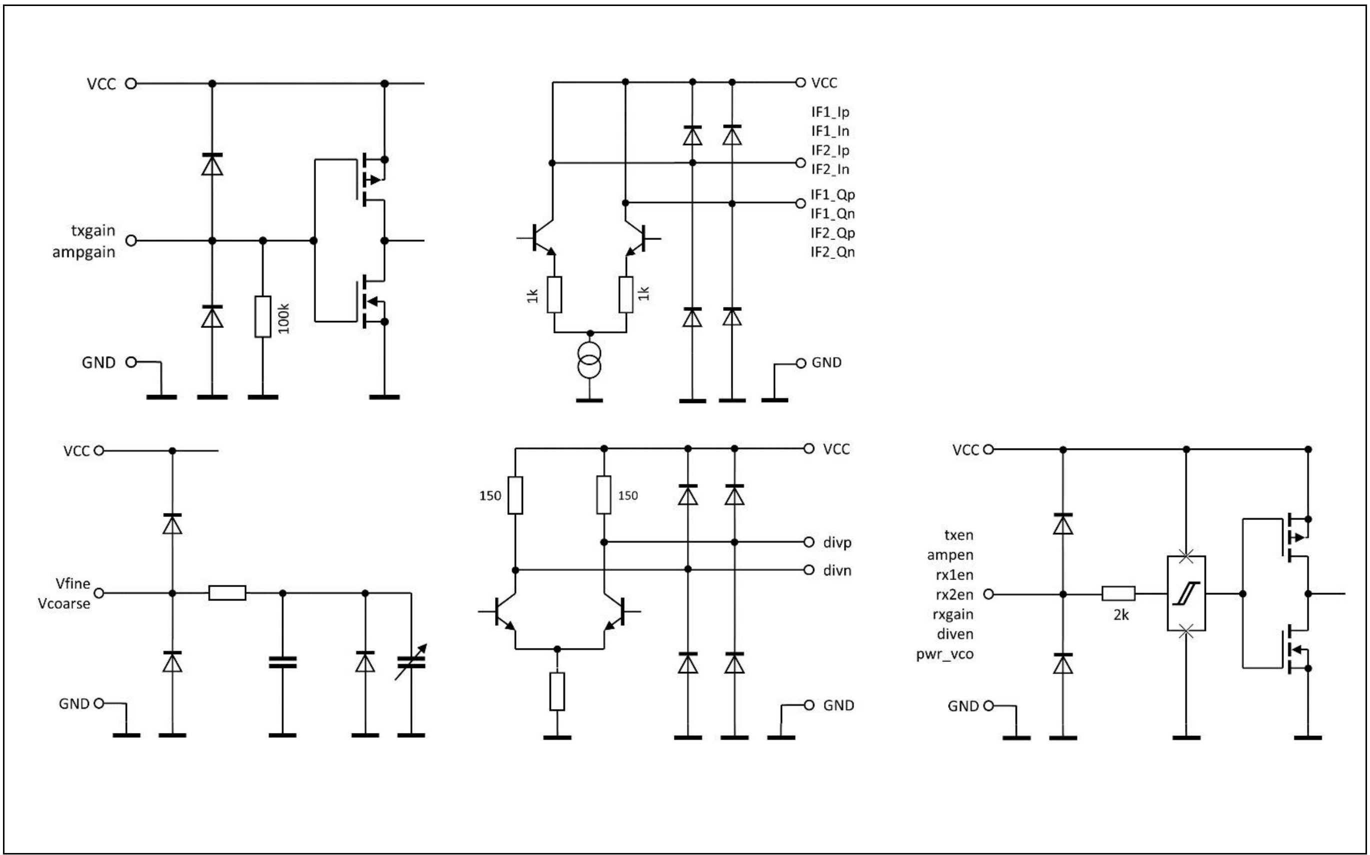


Figure 5 Equivalent I/O Circuits

6.4 VCO Tuning Inputs

The VCO tuning inputs Vfine and Vcoarse are of analog nature but can be switched digitally as well. The tuning inputs differ in their tuning ranges (tuning bandwidth) and slopes, where Vcoarse has wider tuning range, and Vfine, narrower. Unused tuning inputs must be set to a fixed potential (between 0 and V_{CC}). During measurements, Vfine and Vcoarse were shorted together on the test board.

7 Measurement Results

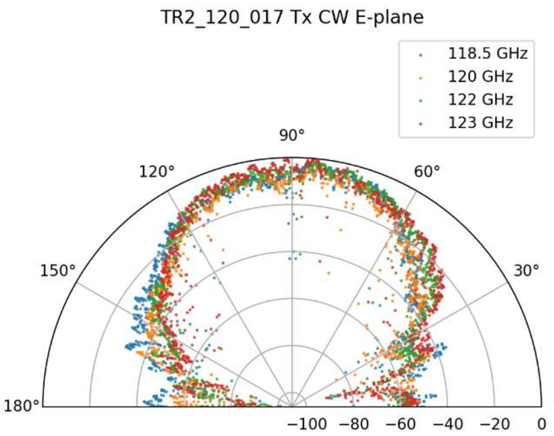


Figure 16: Measured radiation pattern of TX antenna

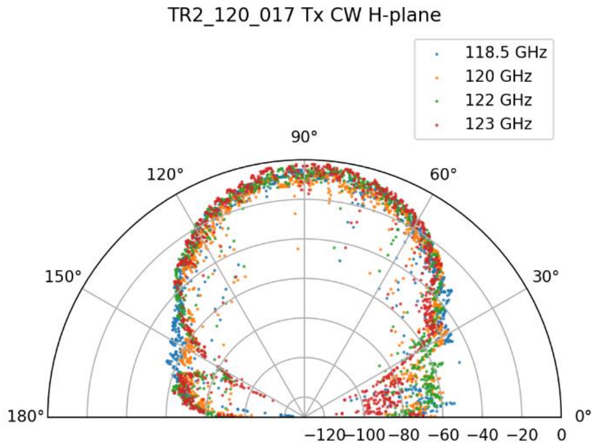


Figure 17: Measured radiation pattern of Tx antenna

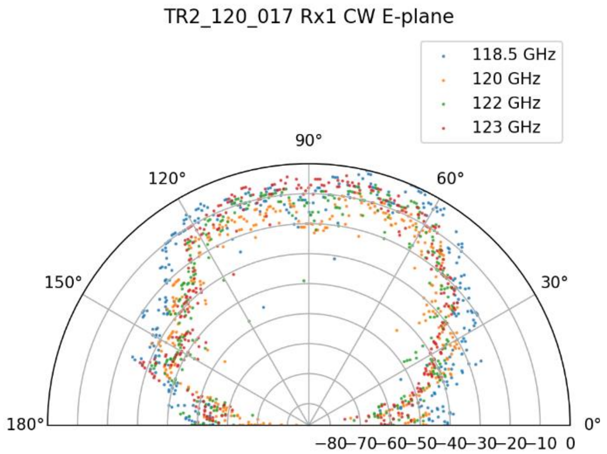


Figure 18: Measured radiation pattern of Rx1 antenna

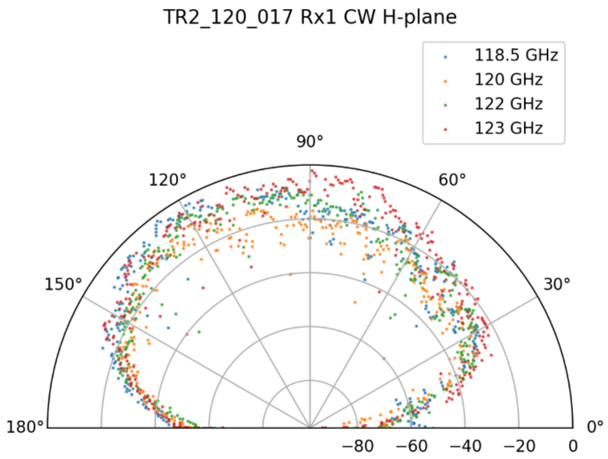


Figure 19: Measured radiation pattern of Rx1 antenna

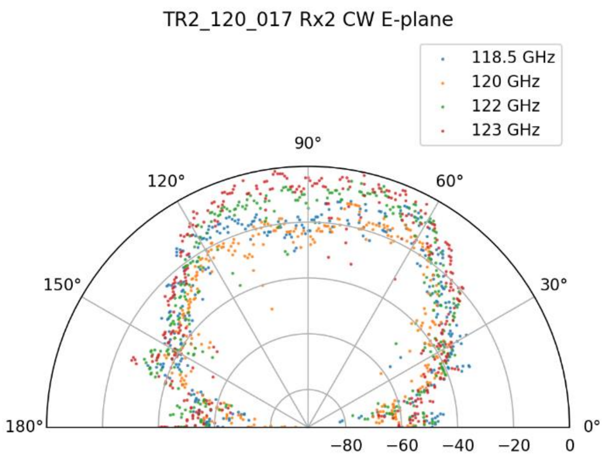


Figure 20: Measured radiation pattern of Rx2 antenna

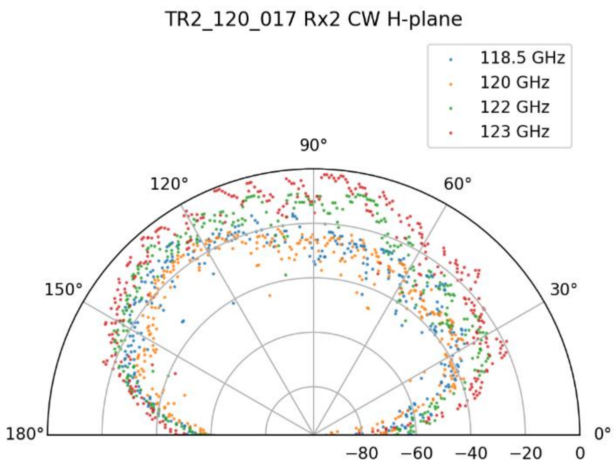


Figure 21: Measured radiation pattern of Rx2 antenna

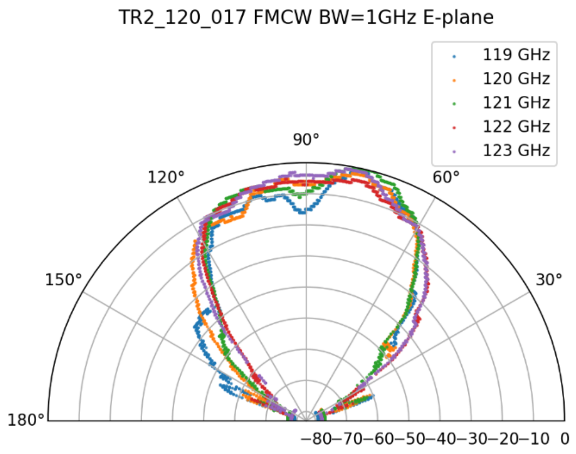


Figure 22: Measured radiation pattern of TX & RX

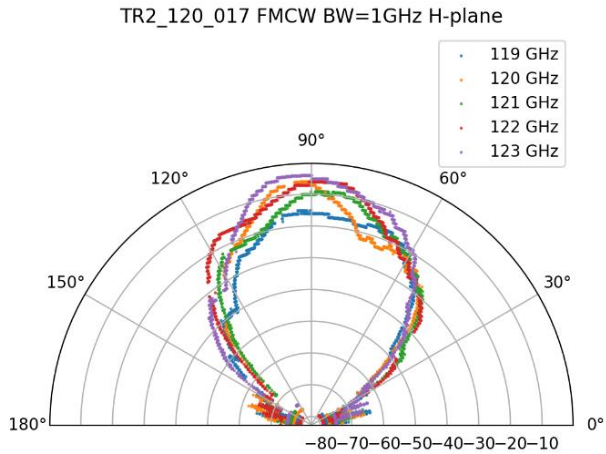


Figure 23: Measured radiation pattern of TX & RX

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