PHYCHIPS

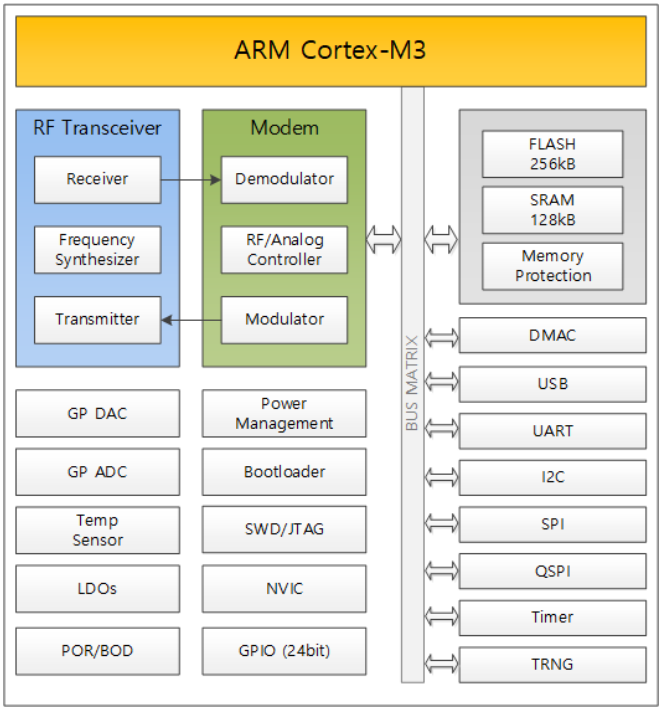
PR7

RAIN RFID Reader SoC

The PR7 is a true single SoC solution for RAIN RFID reader/writer which integrated high performance UHF RF/Analog, MODEM, ARM Cortex-M3 processor, Flash memory and many other features with fully compliant EPC Global Gen2v2/ISO18000-63 protocol. With high integration and excellent performance, it will be a new product that leads the market by being used in various fields ranging from handheld to fixed readers.

Key Feature

- RAIN RFID Reader SoC
- Frequency range: 860 ~ 930MHz
- 3.3V single power supply
- ARM Cortex-M3
- 256KB Embedded Flash
- 128KB SRAM
- PR-ASK, DSB-ASK
- Support DRM
- EPC Gen2v2
- 8mm x 8mm 96-pin LGA package



1. System Overview

1.1 Instruction

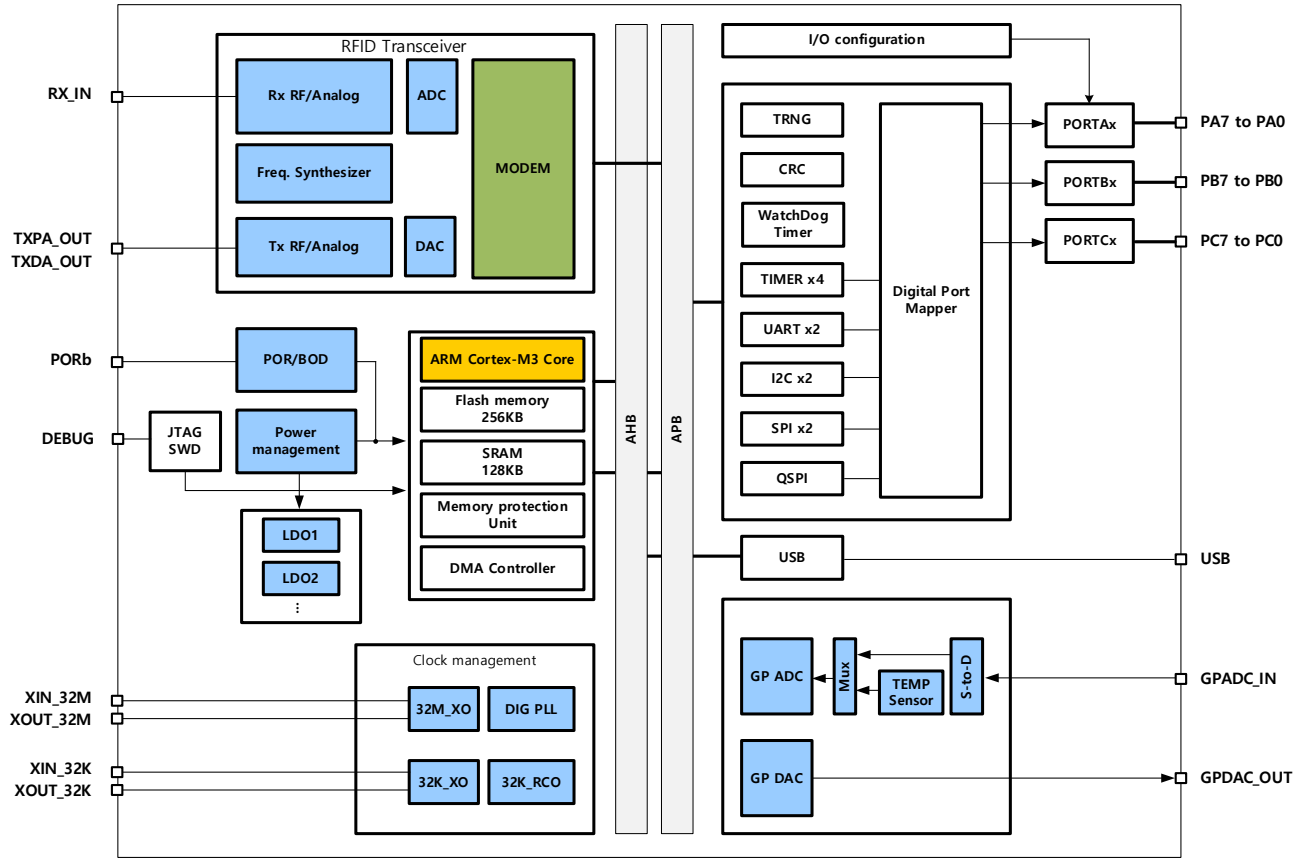


Figure 1 PR7 Overall block diagram

PR7 consolidates RF/Analog, MODEM, and MCU functionalities into a single chip. The RF transceiver employs a direct conversion structure, while the MODEM fully adheres to the EPC gen2v2 air protocol. Additionally, it provides support for various standards based on ISO 18000-6 (ISO18000-62, 18000-63, 18000-64). The chip includes a built-in Power-On Reset (POR) and Brown-Out Detector (BOD), along with an integrated Low Drop-Out (LDO) for core power generation. The MCU is built on the ARM Cortex-M3 architecture, featuring 256 kB of embedded flash and 128 kB of SRAM. It offers support for USB (12Mbps) and various serial interfaces, including UART, I2C, SPI, and QSPI.

The following documents provide additional information.

Firmware Development user manual
Firmware download & debugging manual
WINE Reader Control Protocol manual
WINE API user manual

PR7 reference design

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Condition	Min.	Typ.	Max.	Unit
Supply voltage					V
Storage Temperature		-55		+125	℃
Electrostatic discharge rating (HBM)			2000		V

2.2 Operating conditions

Parameter	Condition	Min.	Typ.	Max.	Unit
Ambient operating temperature		-40		+85	℃
Supply voltage			3.3		V

2.3 Current consumption

Parameter	Mode	Condition	Min.	Typ.	Max.	Unit
PR7 Chip only	Active	CW on, DA on, Tx PA off, LCA min		145		mA
		CW on, DA on, Tx PA 20dBm, LCA min		310		mA
	IDLE	CW off, RF off		35		mA
	SLEEP	CPU sleep		16		mA
	DEEPSLEEP	-		TBD		mA
	STOP	-		TBD		mA

1) Supply voltage: VCC_xx = 3.3V

2.4 Radio Receiver specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Input Frequency		860		930	MHz
Full path gain	In-band gain	18		80	dB
Gain control range			63		dB
Analog filter bandwidth	3dB cut-off frequency	60		1000	kHz

2.5 Radio Transmitter specifications

Parameter	Condition	Min.	Typ.	Max.	Unit
Tx DA output power	@ Max gain		6		dBm
Tx PA output power			21		dBm
Tx PA gain	@ Max gain		20		dB

2.6 Frequency Synthesizer specifications

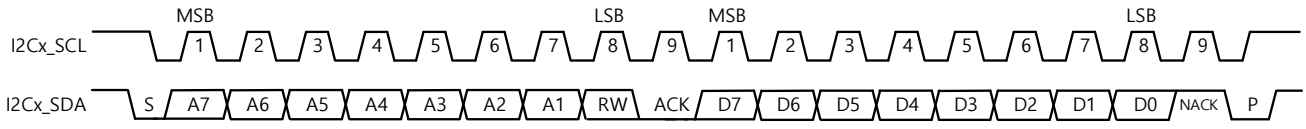
Parameter	Condition	Min.	Typ.	Max.	Unit
Reference clock frequency			32		MHz
Frequency Range		860		930	MHz
Lo phase noise					
@ 10kHz			-67		dBc/Hz
@250kHz			-118		dBc/Hz
@1MHz			-127		dBc/Hz

2.7 Peripheral specifications

TBD

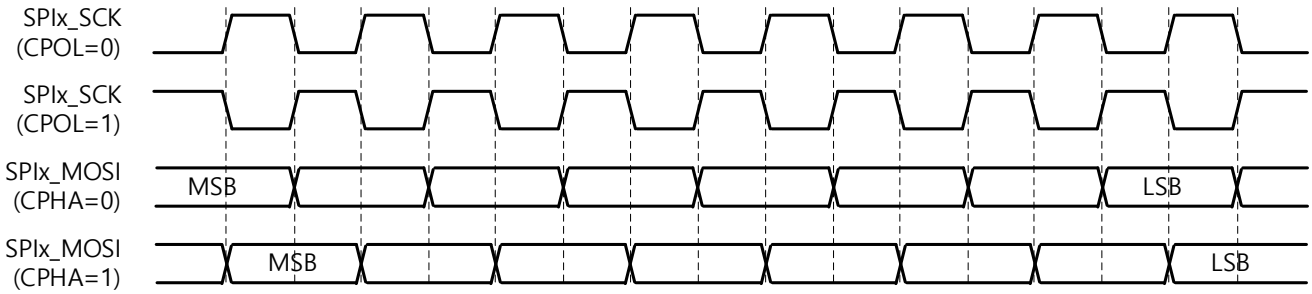
2.8 Timing specifications

2.8.1 I2C



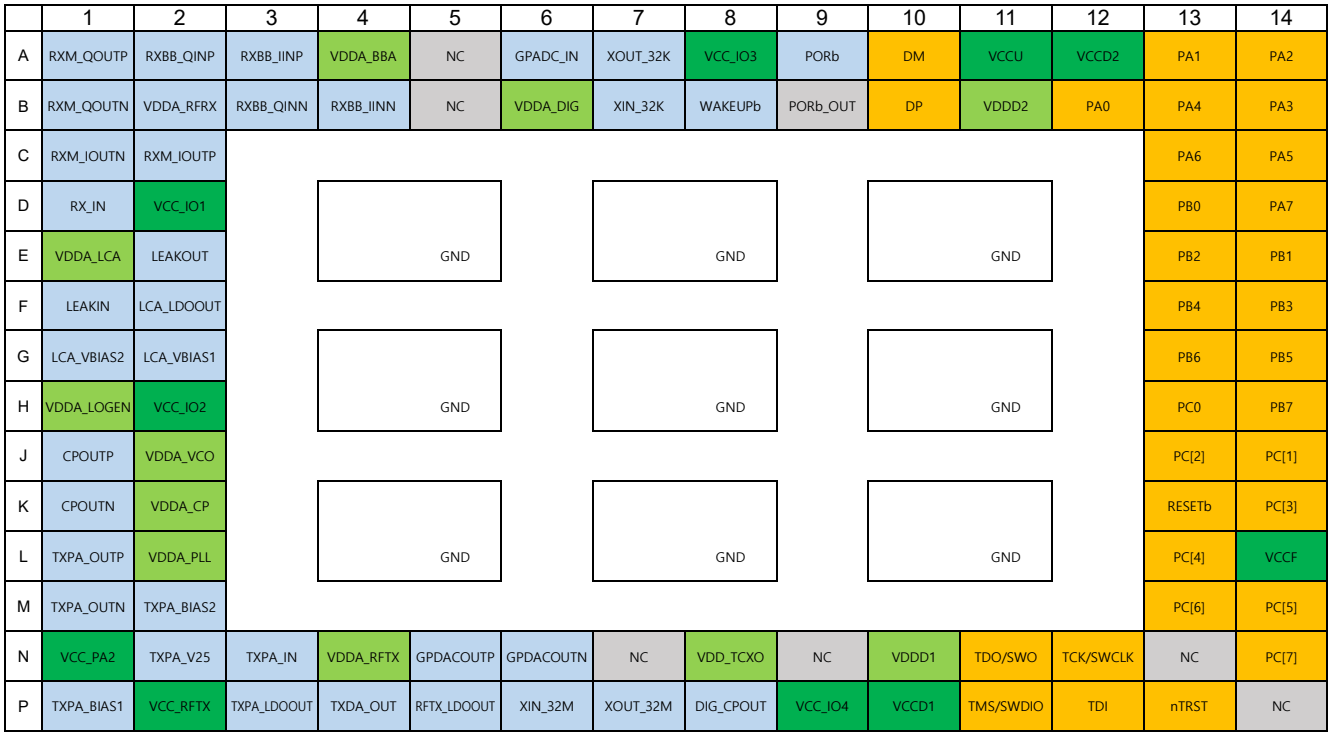
Parameter	Condition	Min.	Typ.	Max.	Unit
I2C_SCL frequency				400	kHz

2.8.2 SPI



Parameter	Condition	Min.	Typ.	Max.	Unit
SPIx_SCK clock frequency	Master			64	MHz

3. Pin description



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	RXM_QOUTP	RXBB_QINP	RXBB_IINP	VDDA_BBA	NC	GPADC_IN	XOUT_32K	VCC_IO3	PORb	DM	VCCU	VCCD2	PA1	PA2
B	RXM_QOUTN	VDDA_RFRX	RXBB_QINN	RXBB_IINN	NC	VDDA_DIG	XIN_32K	WAKEUPb	PORb_OUT	DP	VDDD2	PA0	PA4	PA3
C	RXM_IOUTN	RXM_IOUTP											PA6	PA5
D	RX_IN	VCC_IO1		GND			GND			GND			PB0	PA7
E	VDDA_LCA	LEAKOUT											PB2	PB1
F	LEAKIN	LCA_LDOOUT											PB4	PB3
G	LCA_VBIAS2	LCA_VBIAS1		GND			GND			GND			PB6	PB5
H	VDDA_LOGEN	VCC_IO2											PC0	PB7
J	CPOUTP	VDDA_VCO											PC[2]	PC[1]
K	CPOUTN	VDDA_CP		GND			GND			GND			RESETb	PC[3]
L	TXPA_OUTP	VDDA_PLL											PC[4]	VCCF
M	TXPA_OUTN	TXPA_BIAS2											PC[6]	PC[5]
N	VCC_PA2	TXPA_V25	TXPA_IN	VDDA_RFTX	GPDACOUTP	GPDACOUTN	NC	VDD_TCXO	NC	VDDD1	TDO/SWO	TCK/SWCLK	NC	PC[7]
P	TXPA_BIAS1	VCC_RFTX	TXPA_LDOOUT	TXDA_OUT	RFTX_LDOOUT	XIN_32M	XOUT_32M	DIG_CPOUT	VCC_IO4	VCCD1	TMS/SWDIO	TDI	nTRST	NC

No	Name	IO	Type	Description
A1 B1	RXM_QOUTP RXM_QOUTN	O	Analog	Rx mixer Q path positive/negative output
C1 C2	RXM_IOUTN RXM_IOUTP	O	Analog	Rx mixer I path positive/negative output
A2 B3	RXBB_QINP RXBB_QINN	I	Analog	Rx BBA Q path positive/negative input
A3 B4	RXBB_IINP RXBB_IINN	I	Analog	Rx BBA I path positive/negative input
A4	VDDA_BBA	P	Analog	LDO output for BBA
D2	VCC_IO1	P	Analog	Power supply (IO1)
D1	RX_IN	I	RF	Rx RF input
B2	VDDA_RFRX	P	Analog	LDO output for RF RX
F1	LEAKIN	I	RF	LCA (Leakage Cancellation Amp) input
E2	LEAKOUT	O	RF	LCA (Leakage Cancellation Amp) output
G2	LCA_VBIAS1	O	Analog	LCA voltage bias1: capacitor is required
G1	LCA_VBIAS2	O	Analog	LCA voltage bias2: capacitor is required
E1	VDDA_LCA	P	Analog	LCA DC power input
F2	LCA_LDOOUT	O	Analog	LDO output for LCA: connect to VDDA_LCA

H1	VDDA_LOGEN	P	Analog	LDO output for LO gen
H2	VCC_IO2	P	Analog	Power supply (IO2)
J1 K1	CPOUTP CPOUTN	O	Analog	RFPLL Charge Pump output
J2	VDDA_VCO	P	Analog	LDO output for RFPLL VCO
K2	VDDA_CP	P	Analog	LDO output for RFPLL Charge pump
L2	VDDA_PLL	P	Analog	LDO output for RFPLL Digital
L1 M1	TXPA_OUTP TXPA_OUTN	O	RF	TX Internal Power Amp output
P1 M2	TXPA_BIAS1 TXPA_BIAS2	O	Analog	TX Power Amp Bias1: connect to capacitor TX Power Amp Bias2: connect to capacitor
N3	TXPA_IN	I	RF	Tx Internal Power Amp input
N2	TXPA_V25	O	Analog	DC power input for Power Amp
P3	TXPA_LDOOUT	P	Analog	LDO output for TX PA
N1	VCC_PA2	P	Analog	Power supply (PA)
P2	VCC_RFTX	P	Analog	Power supply (PAIO)
P4	TXDA_OUT	O	RF	TXDA output
N4	VDDA_RFTX	P	Analog	DC power input for RFTX
P5	RFTX_LDOOUT	O	Analog	LDO output for RFTX: connect to VDDA_RFTX
N5 N6	GPDACOUTP GPDACOUTN	O	Analog	GP DAC output
P6	XIN_32M	IO	Analog	X-tal input or TCXO input (32MHz)
P7	XOUT_32M	IO	Analog	X-tal output (32MHz)
P8	DIG_CPOUT	O	Analog	Charge pump output for Digital PLL
N8	VDD_TCXO	P	Analog	LDO output for Digital PLL and TCXO buffer
P9	VCC_IO4	P	Analog	Power supply (IO4)
P10	VCCD1	P	Analog	Power supply (Digital)
N10	VDDD1	P	Analog	LDO output for Digital
N11	TDO/SWO	O	Digital	JTAG Data Out / optional trace output
N12	TCK/SWCLK	I	Digital	JTAG Clock / Serial Wire Clock
P11	TMS/SWDIO	I	Digital	JTAG Test Mode State / Serial Wire Data Input Output
P12	TDI	I	Digital	JTAG Data In pin
P13	nTRST	I	Digital	JTAG reset pin
N14	PC7	IO	Digital	Digital IO: Port C
M13	PC6	IO	Digital	Digital IO: Port C
M14	PC5	IO	Digital	Digital IO: Port C
L13	PC4	IO	Digital	Digital IO: Port C
K14	PC3	IO	Digital	Digital IO: Port C

J13	PC2	IO	Digital	Digital IO: Port C
J14	PC1	IO	Digital	Digital IO: Port C
H13	PC0	IO	Digital	Digital IO: Port C
K13	RESETb	I	Digital	Digital reset pin
L14	VCCF	P	Digital	Power supply (F)
H14	PB7	IO	Digital	Digital IO: Port B
G13	PB6	IO	Digital	Digital IO: Port B
G14	PB5	IO	Digital	Digital IO: Port B
F13	PB4	IO	Digital	Digital IO: Port B
F14	PB3	IO	Digital	Digital IO: Port B
E13	PB2	IO	Digital	Digital IO: Port B
E14	PB1	IO	Digital	Digital IO: Port B
D13	PB0	IO	Digital	Digital IO: Port B
D14	PA7	IO	Digital	Digital IO: Port A
C13	PA6	IO	Digital	Digital IO: Port A
C14	PA5	IO	Digital	Digital IO: Port A
B13	PA4	IO	Digital	Digital IO: Port A
B14	PA3	IO	Digital	Digital IO: Port A
A14	PA2	IO	Digital	Digital IO: Port A
A13	PA1	IO	Digital	Digital IO: Port A
B12	PA0	IO	Digital	Digital IO: Port A
A12	VCCD2	P	Digital	Power supply (digital)
A11	VCCU	P	Digital	Power supply (USB)
B11	VDDD2	P	Digital	LDO output for Digital
B10 A10	DP DM	IO	Digital	USB D+, D-
A9	PORb	I	Analog	Power on Reset Capacitor 1nF should be connected
B9	PORb_OUT	O	Analog	Power on Reset output (for test)
B8	WAKEUPb	I	Analog	Wakeup signal
A8	VCC_IO3	P	Analog	Power supply (IO3)
A7	XOUT_32K	O	Analog	32kHz X-tal buffer output
B7	XIN_32K	I	Analog	32kHz X-tal buffer output
A6	GPADC_IN	I	Analog	GP ADC input
B6	VDDA_DIG	P	Analog	LDO output for ADC and DAC
	NC	-	-	No connected, these pins should be open

4. Functional Description

4.1 RF

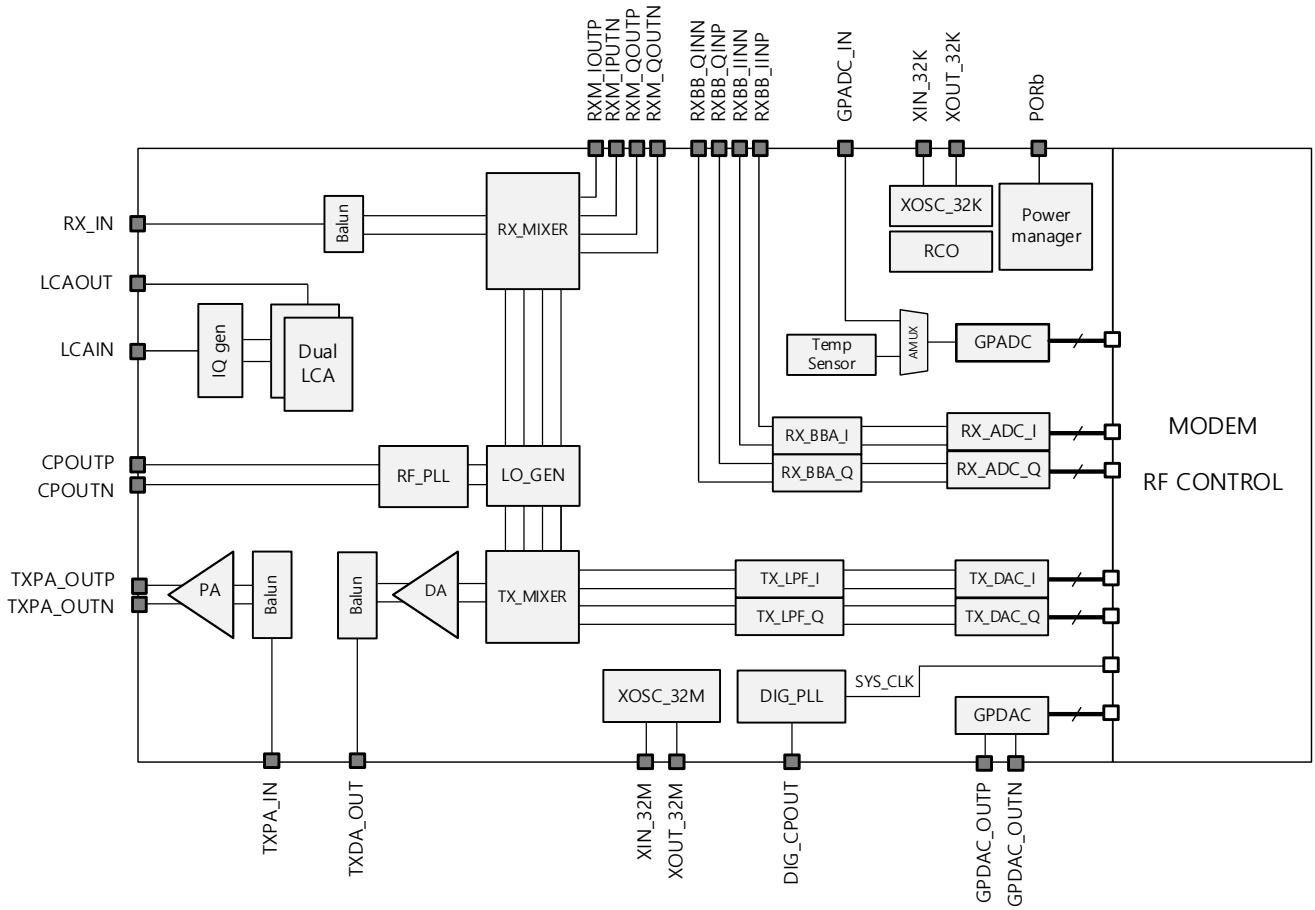


Figure 2 RF block diagram

4.1.1 Receiver path

The receiver consists of a mixer, BBA (Base Band Analog), and ADC. The Rx mixer performs down-conversion of the RF received signal to the Base Band signal. The BBA circuit includes DC offset cancellation, an analog low-pass filter, and a variable gain amplifier. The BBA provides optimized gain, LPF bandwidth, DC cutoff frequency, etc., based on the characteristics of the input signal (magnitude, link frequency, modulation method). The Rx ADC converts the baseband analog signal to a digital signal for the MODEM.

AC coupling or DRM filter is required between the Rx Mixer output (RXM_IOUTP/N, RXM_QOUTP/N) and Rx BBA input (RXBB_IINP/N, RXBB_QIN). The specifications of the DRM filter are provided through a separate application circuit. The PR7 receiver includes a Leakage Cancellation Amplifier (LCA) to eliminate Tx leakage. An additional 3dB coupler is required, effectively removing leakage even in structures with Tx output power of 30dBm or higher. The Dual LCA particularly adapts dynamically to changes in leakage magnitude due to

various antenna S11 (Return loss).

4.1.2 Transmitter path

The PR7 transmitter is composed of a DAC, LPF, mixer, and DA (Driver Amp). The Tx DAC converts the modulated digital baseband signal into an analog signal, and at the Tx mixer, it undergoes up-conversion to a UHF RF signal. To comply with country-specific regulations, appropriate filters (such as SAW filters) may be required at the DA output.

The PR7 includes a built-in Power Amplifier (PA), and the DA output or filter output can be connected to TXPA_IN for use. The internal PA in PR7 requires a balun for diff-to-single conversion, as it provides a differential output. If a higher output power, such as 30dBm or more, is needed, an external PA is required instead of the internal PA.

4.1.3 Frequency synthesizer

The PR7 has two built-in Frequency synthesizers. The RF_PLL, utilizing a Fractional-N structure, provides the LO signal for the Rx mixer or Tx mixer. CP_OUTP and CP_OUTN serve as the input pins for the differential loop filter of RF_PLL. DIG_PLL generates the system clock for the MCU, as well as clocks for the MODEM, ADC, and DAC. The loop filter for DIG_PLL is connected to DIG_CPOUT. A 32MHz reference clock is required for the frequency synthesizer. An oscillator buffer for the 32MHz clock is built-in, providing two methods for supplying the reference clock. The first involves connecting a 32MHz TCXO (or 32MHz Oscillator) to XIN_32M. The second method is connecting a 32MHz Xtal to XIN_32M and XOUT_32M.

PR7 includes a low-frequency clock of 32.768KHz for power management and wakeup time control. For more precise time control, an external 32.768kHz Xtal can be connected to XIN_32K and XOUT_32K for use.

4.1.4 Others

PR7 features a General Purpose ADC and General Purpose DAC. The GP ADC converts the input at GPADC_IN into 12-bit digital data. On the other hand, the GP DAC converts 12-bit digital data into an analog signal and outputs it differentially as GPDAC_OUTP and GPDAC_PUTN.

4.2 MCU

4.2.1 Feature

- Cortex M3 MCU Core (up to 128MHz)
- 256KB embedded Flash memory with flash cache
- 128KB SRAM
- 2 UART with modem control
- 2 SPI Master/Slave
- 2 I2C Master/Slave
- QSPI Master
- 6 Timer / 2 Dual Timer
- Watchdog Timer
- True Random Number Generator (TRNG)
- GPIO (24bit, pullup, driving strength)
- Configurable Port Muxing
- USB Full Speed Device Controller/PHY
- 12-channel AHB DMA

4.2.2 UART

The UART (Universal Asynchronous Receiver/Transmitter) core provides serial communication capabilities, allowing communication with other computers, modems, or external devices using serial cables and the RS-232 protocol. The UART interface is compatible with the industry-standard National Semiconductors' 16550A device. It offers two UARTs, UART0 and UART1, each equipped with built-in transmit FIFO and receive FIFO. All UARTs support hardware control signals, including CTS and RTS, and can be utilized with DMA controllers.

4.2.3 I2C

I2C is a 2-wire bidirectional serial bus that provides a simple and efficient method for devices to exchange data. It is suitable for applications where intermittent communication over short distances between multiple devices is needed. The I2C standard includes collision detection and arbitration mechanisms to prevent data corruption when multiple masters attempt to control the bus simultaneously. Two I2C interfaces, I2C0 and I2C1, are provided, supporting two transmission speeds: Normal Mode (100Kbps) and Fast Mode (400Kbps).

4.2.4 SPI

SPI (Serial Peripheral Interface) provides both full-duplex and simplex communication modes. It supports both Master and Slave modes and is compatible with the SPI standard of Motorola. Two SPI interfaces, SPI0 and SPI1, are provided, each equipped with built-in transmit FIFO and receive FIFO. Both SPI interfaces can be serviced by the DMA controller.

4.2.5 QSPI (Quad-SPI)

Quad SPI provides a serial communication interface using four data lines, utilizing up to six lines including one Chip Select line and one Clock line. It enables parallel data transmission through the four data lines. Operating solely as a master, Quad SPI can be configured to work in Single (similar to conventional SPI) or Dual modes through the QSPI interface. This interface is commonly used with devices that support Quad SPI communication, such as external flash memory or display devices.

4.2.6 USB

USB supports the USB2.0 Full Speed (12Mbps) interface. It can process the USB protocol and operate as a USB device using the host processor. It has eight endpoints that can be configured via software and supports suspend/resume functionality.

4.2.7 Timer

4.2.7.1 Timer 0~1

This is a 32-bit down-counter timer. It is a basic timer that generates an interrupt when the timer counter reaches 0.

4.2.7.2 Timer 2~5

Timers 2 through 5 support two modes: Input Capture and PWM. Each timer is a 32-bit timer with four independent channels. In Capture mode, the timer counts in the direction set when a pulse with the configured polarity is input to the pin. PWM mode allows for various configurations, including Toggle, Pulse, and PWM modes, by setting the pulse count.

4.2.7.3 Dual Timer

The Dual Timer consists of two programmable 32-bit or 16-bit down counters. The timer can be programmed with either a 32-bit or 16-bit counter and one of the timer modes (free-running, periodic, one-shot).

The dual-input timer generates two interrupts and provides access to a 32-bit free-running counter (FRCs). FRCs operate on a common timer clock and have their clock enable inputs. Each FRC has a prescaler that can divide the activated clock speed by 1, 16, or 256, allowing independent control of the counter speed for each FRC through individual clock activation and prescaler use.

- Free-running mode: The counter wraps around to 0 after reaching the value of 0 and continues counting down from the maximum value.
- Periodic mode: The counter generates interrupts at regular intervals, reloading the original value after surpassing 0.
- One-shot mode: The counter generates an interrupt once and stops until reprogrammed when it reaches 0.

4.2.8 Watchdog timer

The Watchdog Timer is based on a 32-bit down-counter. The Watchdog module generates a regular interrupt based on a programmed value. It monitors the interrupts, and if the counter reaches 0 and stops without the interrupt being cleared, it asserts a reset signal. If the interrupt is not cleared until the counter reaches 0, the watchdog module will re-specify the reset signal. The Watchdog module provides a way to apply a system reset in case of software errors, allowing recovery from software crashes. The watchdog unit can be enabled or disabled as needed.

4.2.9 DMA

DMA (Direct Memory Access) is used to replace CPU functions, such as memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. It provides up to 12 DMA channels and can be utilized for controlling peripherals like UART and SPI.

4.2.10 TRNG (True Random Number Generator)

Using TRNG (True Random Number Generator) allows the generation of a random bit stream. TRNG provides full entropy output to the application in 32-bit samples. It is utilized during Frequency Hopping to randomly generate sequences for frequency channels.

4.2.11 Debug Mode

The ARM SWJ-DP interface is integrated to provide a combined JTAG and SWD debug port. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and specific sequences on the TMS pin are used to switch between JTAG-DP and SW-DP. Debugging can be controlled through the JTAG/SWD access port using debugging tools.

4.2.12 GPIO

GPIO (General Purpose Input/Output) is a general-purpose I/O interface unit that provides a total of 24 pins. It offers programmable interrupt generation capabilities and supports bit masking using address values. The masked access feature allows reading or writing individual bits or multiple bits in a single transaction. Additionally, it supports pin multiplexing, enabling the switch to alternative functions.

4.2.13 Interrupt

IRQ No	Type	IRQ No	Type
0	Reserved	33	Embedded Flash
2	Reserved	34	Flash Cache
5	RTC	44	TRNG
6	All GPIO	45	UART0
8	Timer0	46	UART1
9	Timer1	47	I2C0
10	Dual Timer	48	I2C1
12	Reserved	49	SPI0
16	GPIO A Pin 0	50	SPI1
17	GPIO A Pin 1	51	QSPI
18	GPIO A Pin 2	52	TIMER2
19	GPIO A Pin 3	53	TIMER3
20	GPIO A Pin 4	54	TIMER4
21	GPIO A Pin 5	55	TIMER5
22	GPIO A Pin 6	56	DMA
23	GPIO A Pin 7	57	USB
24	GPIO B Pin 0	60	GPIO C Pin 0
25	GPIO B Pin 1	61	GPIO C Pin 1
26	GPIO B Pin 2	62	GPIO C Pin 2
27	GPIO B Pin 3	63	GPIO C Pin 3
28	GPIO B Pin 4	64	GPIO C Pin 4
29	GPIO B Pin 5	65	GPIO C Pin 5
30	GPIO B Pin 6	66	GPIO C Pin 6
31	GPIO B Pin 7	67	GPIO C Pin 7
32	System Error		

4.2.14 Memory Organization

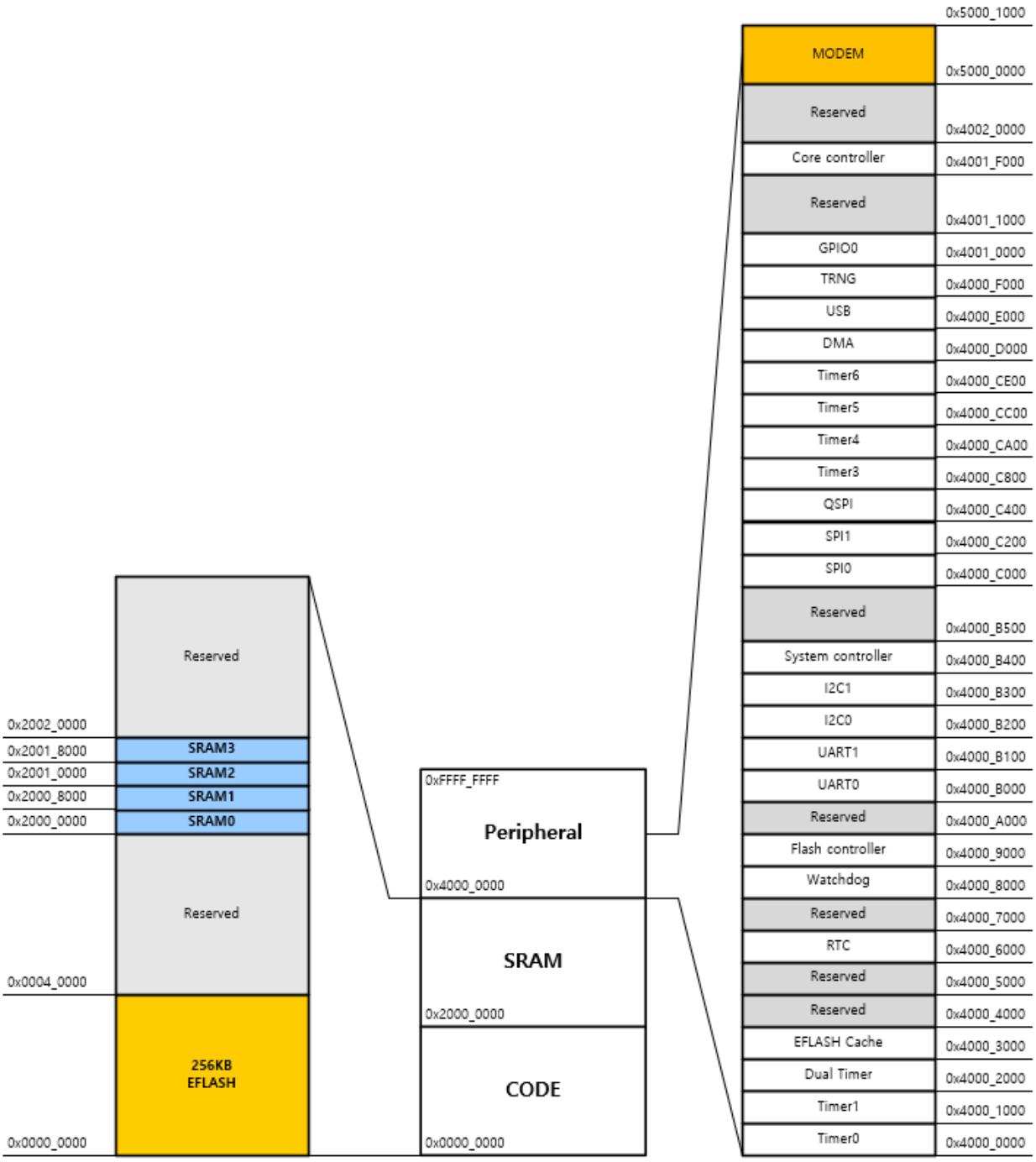


Figure 3 Memory map

4.2.15 Port Map

The PR7 has 3 x 8bit digital IOs, and each IO supports an alternative function that can be selected from UART, I2C, SPI, QSPI, timer, etc.

4.2.15.1 Port A

Port		AF1	AF2	AF3	AF4	AF5
Port A	PA0	UART0_TXD	-	SPI0_CLK	QSPI_CLK	TIM2_CH0
	PA1	UART0_RXD	-	SPI0_CS	QSPI_CS	TIM2_CH1
	PA2	UART0_RTS	I2C0_SCL	SPI0_MISO	QSPI_D0	TIM2_CH2
	PA3	UART0_CTS	I2C0_SDA	SPI0_MOSI	QSPI_D1	TIM2_CH3
	PA4	UART1_TXD	-	SPI1_CLK	QSPI_D2	TIM3_CH0
	PA5	UART1_RXD	-	SPI1_CS	QSPI_D3	TIM3_CH1
	PA6	UART1_RTS	I2C1_SCL	SPI1_MISO	-	TIM3_CH2
	PA7	UART1_CTS	I2C1_SDA	SPI1_MOSI	-	TIM3_CH3

4.2.15.2 Port B

Port		AF1	AF2	AF3	AF4	AF5
Port B	PB0	UART0_TXD	-	SPI0_CLK	QSPI_CLK	TIM2_CH0
	PB1	UART0_RXD	-	SPI0_CS	QSPI_CS	TIM2_CH1
	PB2	UART0_RTS	I2C0_SCL	SPI0_MISO	QSPI_D0	TIM2_CH2
	PB3	UART0_CTS	I2C0_SDA	SPI0_MOSI	QSPI_D1	TIM2_CH3
	PB4	UART1_TXD	-	SPI1_CLK	QSPI_D2	TIM3_CH0
	PB5	UART1_RXD	-	SPI1_CS	QSPI_D3	TIM3_CH1
	PB6	UART1_RTS	I2C1_SCL	SPI1_MISO	-	TIM3_CH2
	PB7	UART1_CTS	I2C1_SDA	SPI1_MOSI	-	TIM3_CH3

4.2.15.3 Port C

Port		AF1	AF2	AF3	AF4	AF5
Port C	PC0	UART0_TXD	-	SPI0_CLK	QSPI_CLK	TIM4_CH0
	PC1	UART0_RXD	-	SPI0_CS	QSPI_CS	TIM4_CH1
	PC2	UART0_RTS	I2C0_SCL	SPI0_MISO	QSPI_D0	TIM4_CH2
	PC3	UART0_CTS	I2C0_SDA	SPI0_MOSI	QSPI_D1	TIM4_CH3
	PC4	UART1_TXD	-	SPI1_CLK	QSPI_D2	TIM5_CH0
	PC5	UART1_RXD	-	SPI1_CS	QSPI_D3	TIM5_CH1
	PC6	UART1_RTS	I2C1_SCL	SPI1_MISO	-	TIM5_CH2
	PC7	UART1_CTS	I2C1_SDA	SPI1_MOSI	-	TIM5_CH3

5. System Control

5.1 Operation mode

PR7 has five operating modes.

5.1.1 IDLE mode

After the Power On Reset (POR), PR7 enters the IDLE mode. The IDLE mode serves as a preparation stage for transitioning to the ACTIVE mode in response to commands from the HOST. In the ACTIVE mode, tag read/write operations are performed. Once the requested commands are executed, PR7 returns to the IDLE mode.

5.1.2 ACTIVE mode

This is the mode in which PR7 performs tag read/write operations. In fact, all commands related to UHF RFID are executed in this mode. The transition from the IDLE mode to the ACTIVE mode can occur either through commands from the HOST via the serial interface or automatically through firmware automation routines.

5.1.3 SLEEP mode

This is the mode in which the MCU enters a sleep state from the IDLE mode. In the SLEEP mode, various peripherals controlled by the MCU can have their clocks controlled to reduce current consumption. The transition to the IDLE mode is triggered by an external interrupt.

5.1.4 DEEPSLEEP mode

After entering the DEEPSLEEP mode, PR7 will wake up and return to the IDLE mode after a user-defined time has elapsed. During the DEEPSLEEP mode, all blocks except the 32.768kHz low-frequency oscillator and counter are turned off to minimize power consumption. There are two methods for waking up from the DEEPSLEEP mode. The first method involves pulling the WAKEUPb pin low, while the second method entails setting a wakeup timer to wake up the system after a specified time.

5.1.5 STOP mode

In the STOP mode, all blocks of PR7 are turned off, and it can only be awakened by the WAKEUPb pin.

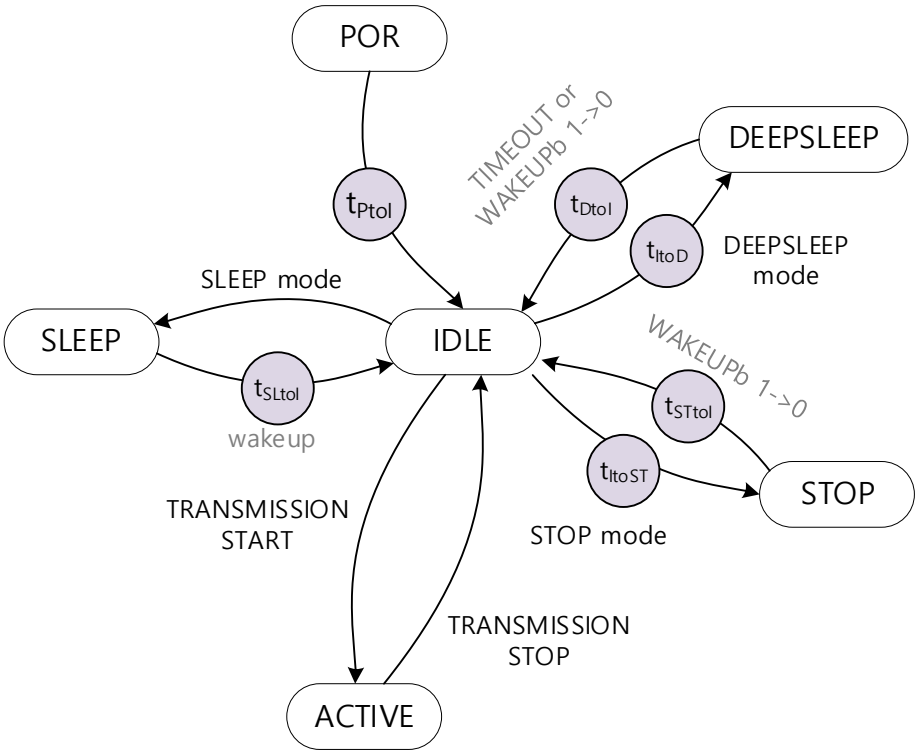


Figure 4 operation mode

Parameter	Condition	Min.	Typ.	Max.	Unit
POR to IDLE time (t_{PtoI})	Time from Reset to entering IDLE mode		13		ms
SLEEP to IDLE time (t_{StoI})	Wake up time from SLEEP mode to IDLE mode		400		ns
IDLE to DEEPSLEEP time (t_{ItoD})	Time from IDLE mode to DEEPSLEEP mode		220		us
DEEPSLEEP to IDLE time (t_{DtoI})	Wakeup time from DEEPSLEEP mode to IDLE mode		16		ms
IDLE to STOP time (t_{ItoST})	Time from IDLE mode to STOP mode		250		us
STOP to IDLE time (t_{STtoI})	Wakeup time from STOP mode to IDLE mode		15		ms

[NOTE] Refer to the WINE reader control protocol for information on the operating method of the mode control

6. Power up timing

PR7 has an internal power management circuit. For the Power On Reset (POR) operation, the following configuration is required. Firstly, a 1nF capacitor is needed on the PORb pin for the reset timing of the POR block. The Power On Reset signal (PORb_OUT) generated by the power management circuit should be connected to the RESETb pin through an RC delay and an AND gate.

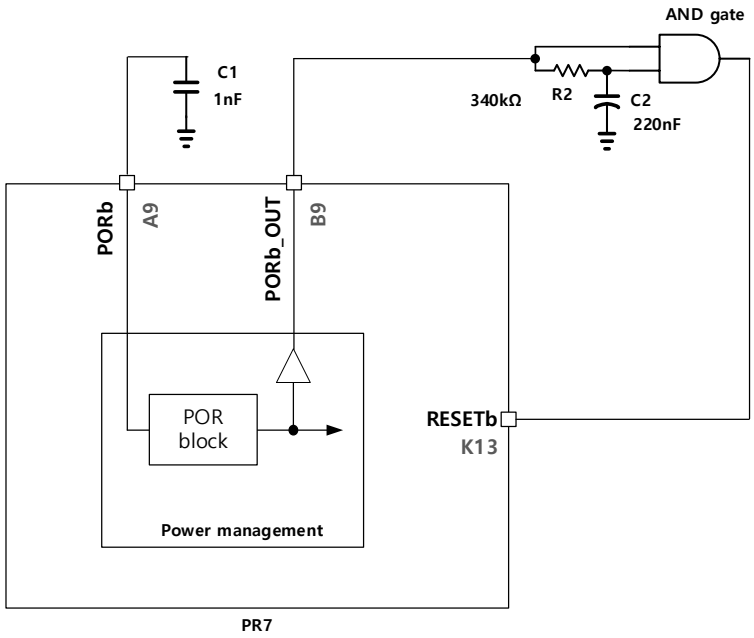


Figure 5 Reset circuit

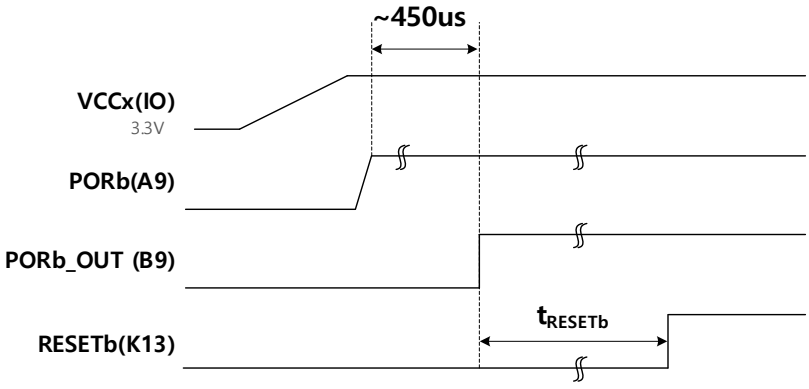


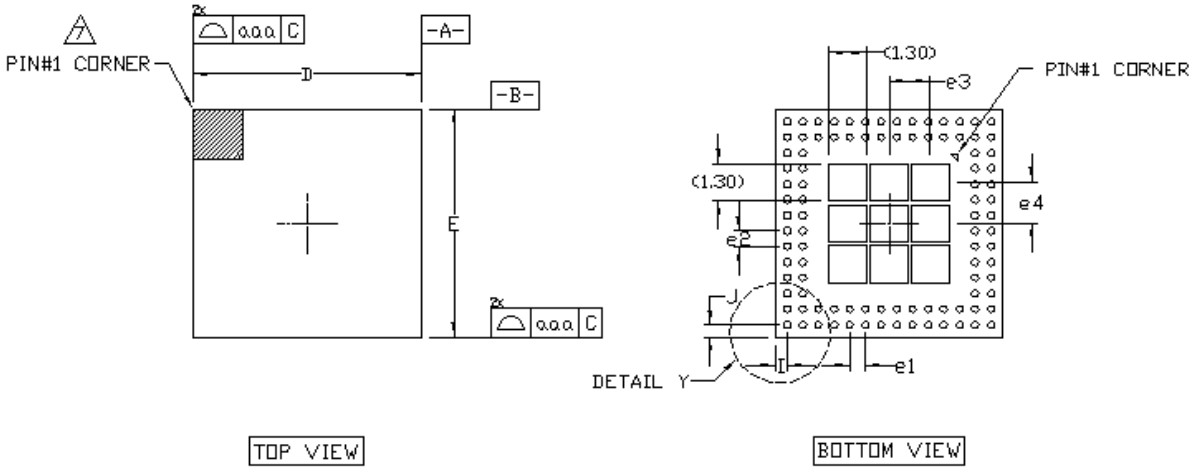
Figure 6 Reset timing

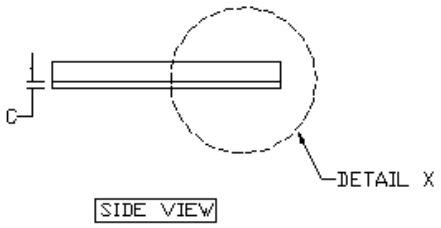
The requirements for t_{RESETb} are as specified in the table below, and to meet these requirements, you can choose the values for R2 and C2

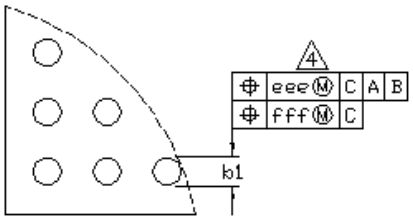
Parameter	Condition	Min.	Typ.	Max.	Unit
Rising edge of PORb to Rising RESETb		40			ms

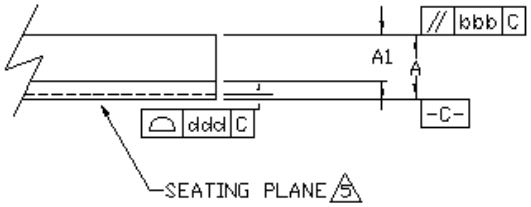
7. Package Information

7.1 Package Dimensions







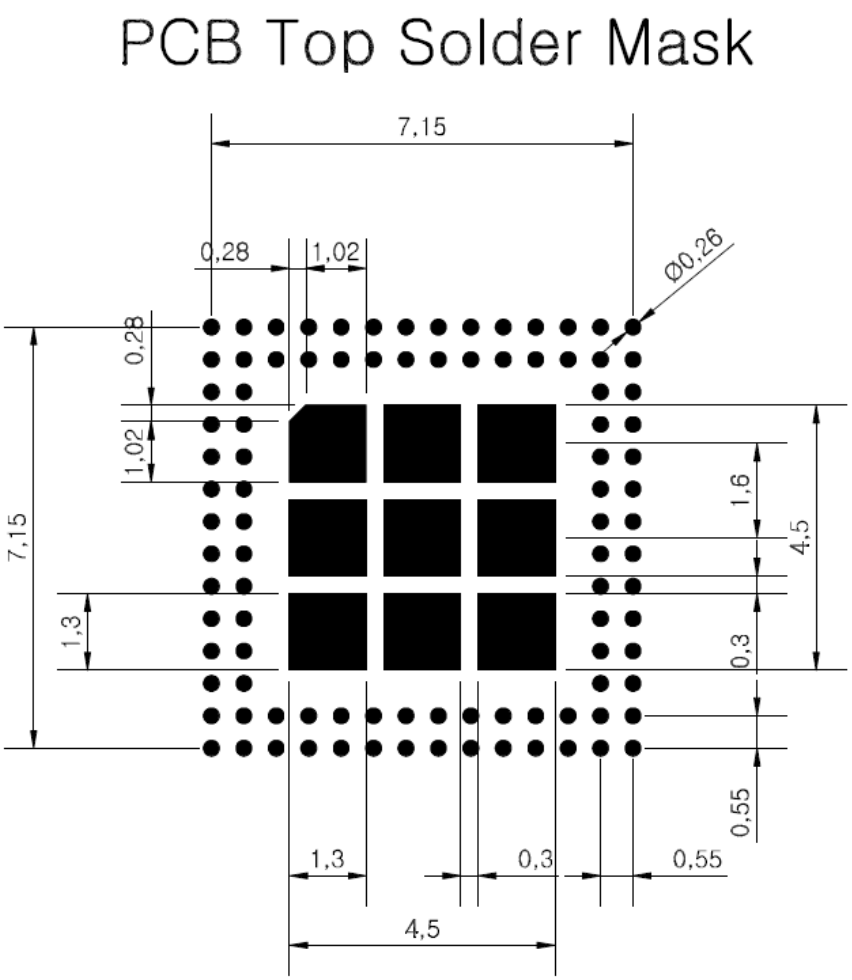


NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC LAND GRID PITCH.
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
4. DIMENSIONS "b" IS MEASURED AT THE MAXIMUM LAND DIAMETER, PARALLEL TO PRIMARY DATUM -C- .
5. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFIND BY THE BOTTOM PACKAGE SURFACE FOR CLARITY.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
7. A1 CORNER MUST BE IDENTIFIED BY INK OR LASER MARK.
8. PACKAGE DIMENSIONS IS ON THE BASE OF JEDEC REGISTRATION 4.25.

SYMBOL	MIN.	NOM.	MAX.
A	0.86	0.91	0.96
A1		0.70 REF.	
D	7.90	8.00	8.10
E	7.90	8.00	8.10
I		0.425 REF.	
J		0.425 REF.	
aaa			0.15
bbb			0.10
ddd			0.10
eee			0.15
fff			0.05
b1		0.25 REF.	
e1		0.55 BSC.	
e2		0.55 BSC.	
e3		1.45 BSC.	
e4		1.45 BSC.	
c		0.21 REF.	

7.2 PCB layout



[unit: mm]

8. Revision History

Version	Date	Page	Description
0.1.0	2024.1.29	-	First edition
0.1.1	2024.1.30		Updated measurement data