

1. Product profile

1.1 General description

Based on Advanced Rugged Technology (ART), this 1900 W LDMOS RF power transistor has been designed to cover a wide range of applications for ISM, broadcast and communications. The unmatched transistor has a frequency range of 1 MHz to 500 MHz.

Table 1. Application information

Test signal	f	V _{DS}	P _L	G _p	η _D
	(MHz)	(V)	(W)	(dB)	(%)
CW pulsed [1][2]	108	50	1700	27.7	74.7
CW pulsed [1][3]	225	55	1900	25.0	75.0

[1] Test circuit.

[2] $t_p = 100 \mu\text{s}$; $\delta = 20 \%$.

[3] $t_p = 100 \mu\text{s}$; $\delta = 10 \%$.

1.2 Features and benefits

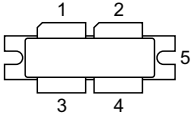
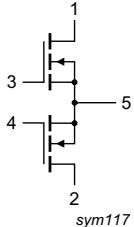
- High breakdown voltage enables class E operation at $V_{DS} = 48 \text{ V}$
- Suitable for $V_{DS} = 50 \text{ V}$ and $V_{DS} = 55 \text{ V}$
- Qualified up to a maximum of $V_{DS} = 55 \text{ V}$
- Characterized from 30 V to 55 V to support a wide range of applications
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness with no device degradation
- High efficiency
- Excellent thermal stability
- Designed for broadband operation
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial, scientific and medical applications
 - ◆ Plasma generators
 - ◆ MRI systems
 - ◆ CO₂ lasers
 - ◆ Particle accelerators
- Broadcast
 - ◆ FM radio
 - ◆ VHF TV
- Communications
 - ◆ Non cellular communications
 - ◆ UHF radar

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source ^[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT539A	ART1K9FHU	9349 607 43112	Tray; 20-fold; non-dry pack	60

4. Limiting values

Table 4. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	177	V
V_{GS}	gate-source voltage		-9	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature ^[1]		-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

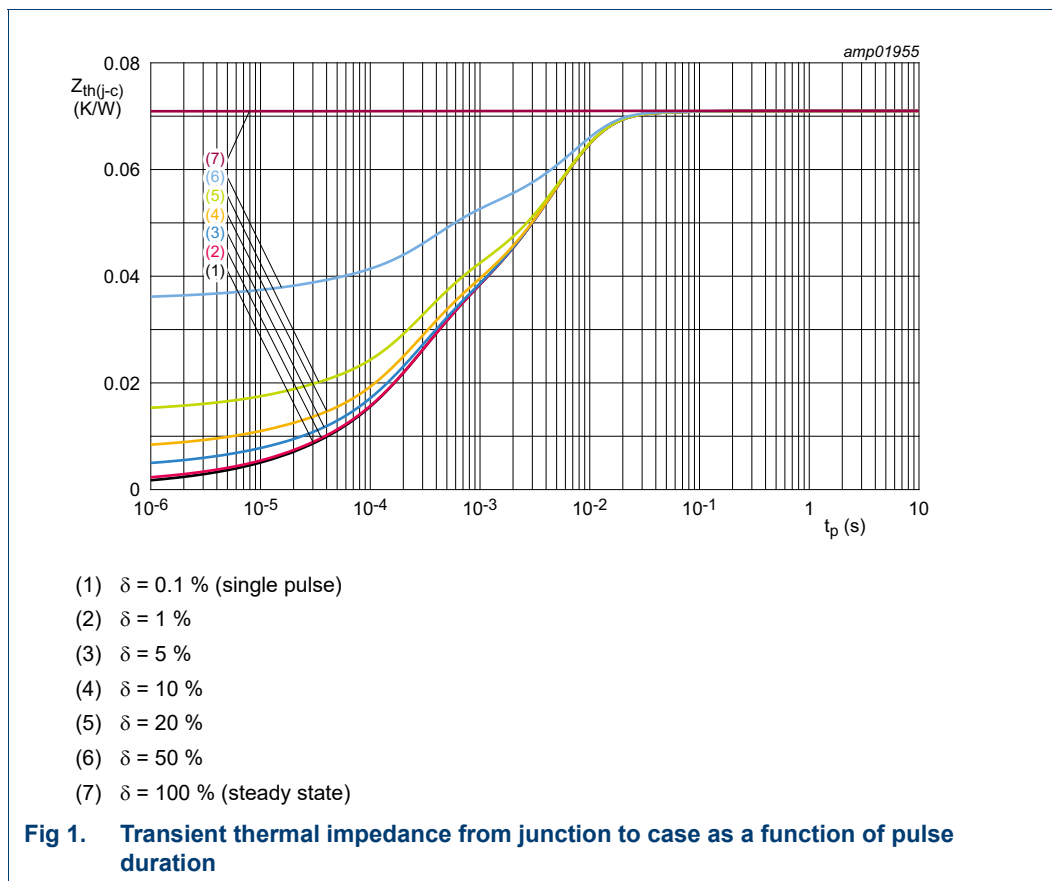
Table 5. Thermal characteristics

According to standard MIL-STD-883E.

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_j = 68\text{ °C}$, measured under RF condition ^{[1][2]}	0.071	K/W

[1] Refer to application note AN221014 on the Ampleon website.

[2] See [Figure 1](#).



6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 6.8\text{ mA}$	177	191	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 20\text{ V}$; $I_D = 675\text{ mA}$	1.6	2.1	2.6	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 55\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 20\text{ V}$	-	>90	-	A
I_{GSS}	gate leakage current	$V_{GS} = 13\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 23.65\text{ A}$	-	0.069	-	Ω

Table 7. AC characteristics
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _{rs}	feedback capacitance	V _{GS} = 0 V; f = 1 MHz				
		V _{DS} = 50 V	-	1.77	-	pF
		V _{DS} = 55 V	-	1.71	-	pF
C _{iss}	input capacitance	V _{GS} = 0 V; f = 1 MHz				
		V _{DS} = 50 V	-	734	-	pF
		V _{DS} = 55 V	-	734	-	pF
C _{oss}	output capacitance	V _{GS} = 0 V; f = 1 MHz				
		V _{DS} = 50 V	-	211	-	pF
		V _{DS} = 55 V	-	201	-	pF

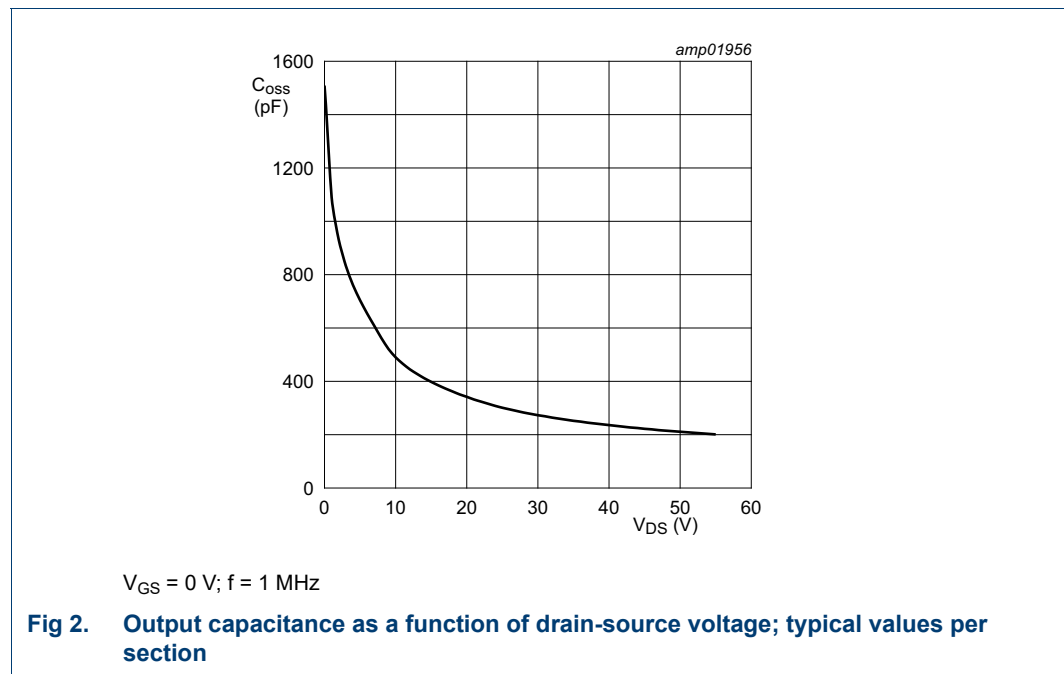


Table 8. RF characteristics
Test signal: pulsed RF; t_p = 100 μs; δ = 5 %; f = 225 MHz; RF performance at V_{DS} = 55 V; I_{Dq} = 50 mA per section; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G _p	power gain	P _L = 1900 W	23.5	24.6	-	dB
RL _{in}	input return loss	P _L = 1900 W	-	-19	-	dB
η _D	drain efficiency	P _L = 1900 W	68	72.5	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The ART1K9FH is capable of withstanding a load mismatch corresponding to $V_{SWR} \geq 65 : 1$ through all phases under the following conditions: $P_L = 1700 \text{ W}$ pulsed at $V_{DS} = 50 \text{ V}$ and $P_L = 1900 \text{ W}$ pulsed at $V_{DS} = 55 \text{ V}$; $I_{DQ} = 100 \text{ mA}$ per section; $t_p = 100 \mu\text{s}$; $\delta = 10 \%$; $f = 225 \text{ MHz}$.

7.2 Impedance information

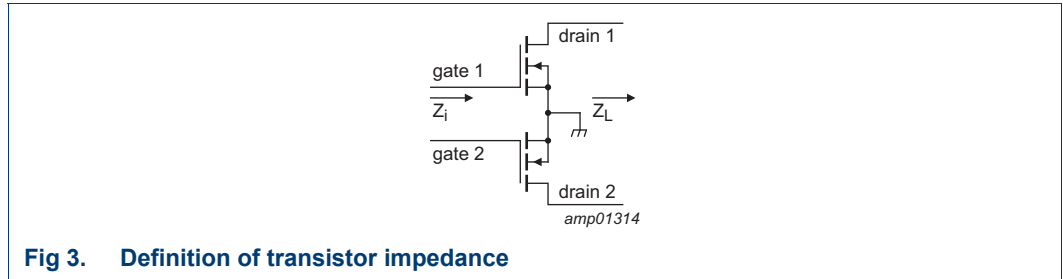


Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance.

f (MHz)	Z_i (Ω)	Z_L (Ω)	P_L (W)
$V_{DS} = 50 \text{ V}$			
225	$0.8 - j3.7$	$2.3 + j0.8$	1700
$V_{DS} = 55 \text{ V}$			
225	$0.8 - j3.7$	$2.4 + j0.9$	1900

7.3 Test circuit

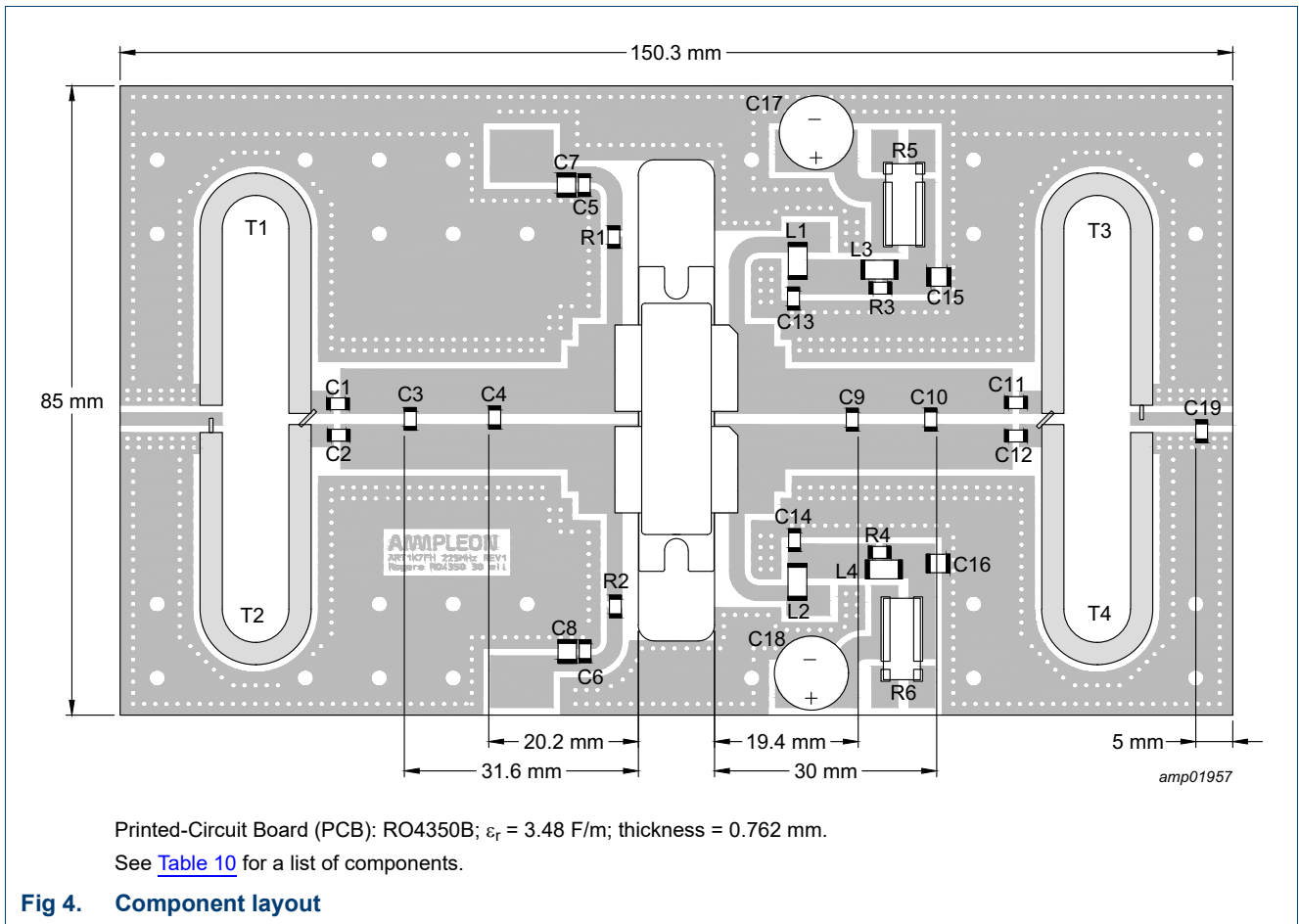


Table 10. List of components

For test circuit see [Figure 4](#).

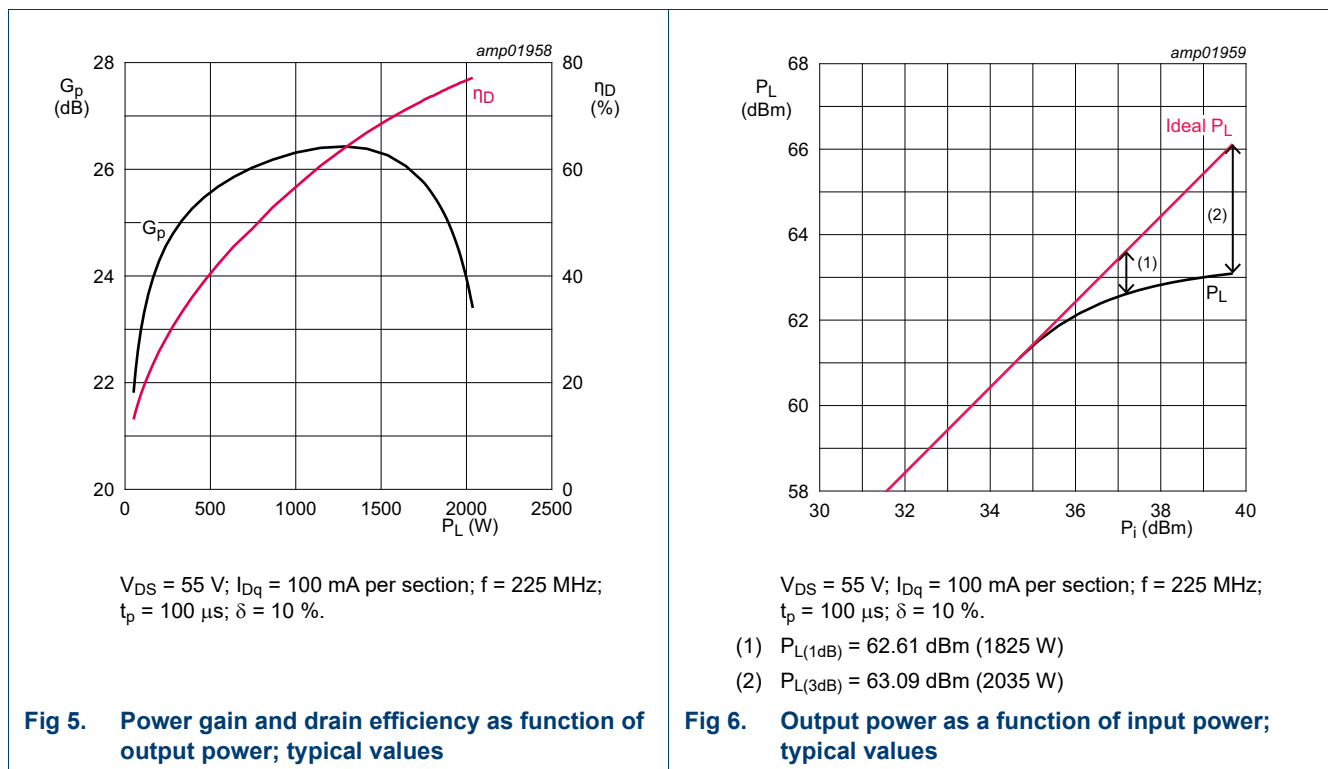
Component	Description	Value	Remarks
C1, C2, C10, C11, C12	multilayer ceramic chip capacitor	47 pF	[1] [2]
C3	multilayer ceramic chip capacitor	100 pF	[1] [2]
C4	multilayer ceramic chip capacitor	160 pF	[1] [2]
C5, C6, C13, C14	multilayer ceramic chip capacitor	620 pF	[1] [2]
C7, C8	multilayer ceramic chip capacitor	4.7 μ F, 100 V	Murata: GRM31CC72A475KE11L
C9	multilayer ceramic chip capacitor	75 pF	[1] [2]
C15, C16	multilayer ceramic chip capacitor	4.7 μ F, 100 V	TDK: CGA9N2X7R2A465K230
C17, C18	electrolytic capacitor	2200 μ F, 100 V	
C19	multilayer ceramic chip capacitor	5.1 pF	[1] [2]
L1, L2	air inductor	33 nH	Coilcraft: 1812SMS-33NGL
L3, L4	air inductor	82 nH	Coilcraft: 1812SMS-82NGL
R1, R2	resistor	510 Ω	SMD 1206

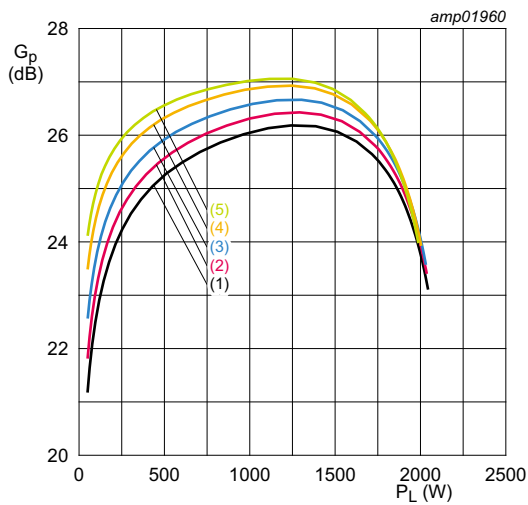
Table 10. List of components ...continued
For test circuit see [Figure 4](#).

Component	Description	Value	Remarks
R3, R4	resistor	5 Ω, 2 x 10 Ω in parallel	SMD 1206
R5, R6	resistor	0.01 Ω	FC4L110R010FER
T1, T2, T3, T4	semi rigid coax	50 Ω, 68 mm	Sucoform 141

- [1] American Technical Ceramics type 800B or capacitor of same quality.
- [2] Vertical mounted.

7.4 Graphical data

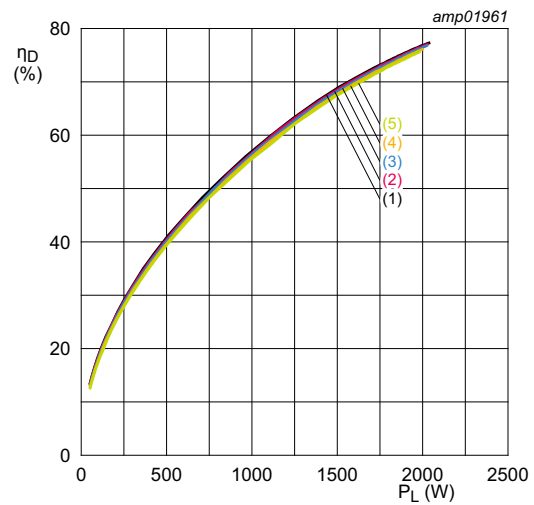




$V_{DS} = 55 \text{ V}$; $f = 225 \text{ MHz}$; $t_p = 100 \text{ }\mu\text{s}$; $\delta = 10 \text{ \%}$.

- (1) $I_{Dq} = 50 \text{ mA}$ per section
- (2) $I_{Dq} = 100 \text{ mA}$ per section
- (3) $I_{Dq} = 200 \text{ mA}$ per section
- (4) $I_{Dq} = 400 \text{ mA}$ per section
- (5) $I_{Dq} = 600 \text{ mA}$ per section

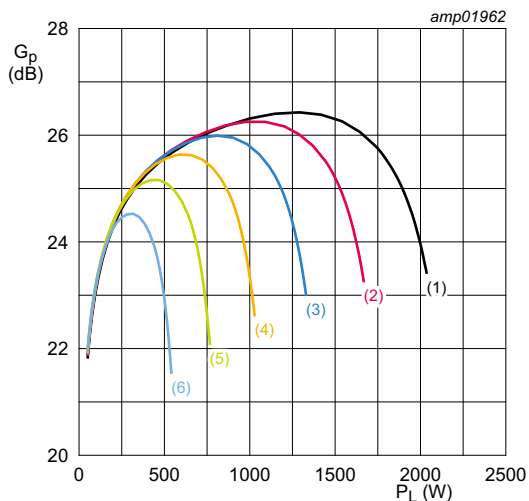
Fig 7. Power gain as a function of output power; typical values



$V_{DS} = 55 \text{ V}$; $f = 225 \text{ MHz}$; $t_p = 100 \text{ }\mu\text{s}$; $\delta = 10 \text{ \%}$.

- (1) $I_{Dq} = 50 \text{ mA}$ per section
- (2) $I_{Dq} = 100 \text{ mA}$ per section
- (3) $I_{Dq} = 200 \text{ mA}$ per section
- (4) $I_{Dq} = 400 \text{ mA}$ per section
- (5) $I_{Dq} = 600 \text{ mA}$ per section

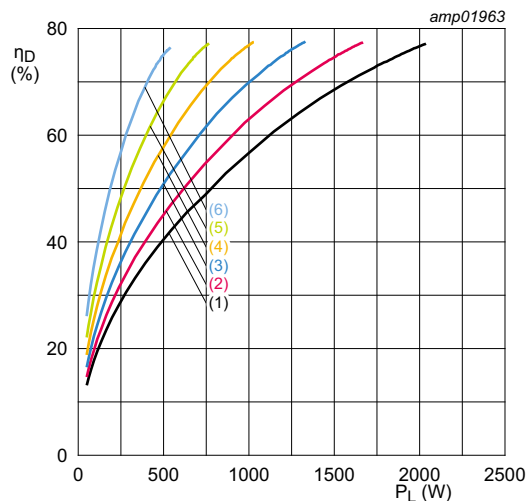
Fig 8. Drain efficiency as a function of output power; typical values



$I_{Dq} = 100$ mA per section; $f = 225$ MHz; $t_p = 100$ μ s;
 $\delta = 10$ %.

- (1) $V_{DS} = 55$ V
- (2) $V_{DS} = 50$ V
- (3) $V_{DS} = 45$ V
- (4) $V_{DS} = 40$ V
- (5) $V_{DS} = 35$ V
- (6) $V_{DS} = 30$ V

Fig 9. Power gain as a function of output power; typical values



$I_{Dq} = 100$ mA per section; $f = 225$ MHz; $t_p = 100$ μ s;
 $\delta = 10$ %.

- (1) $V_{DS} = 55$ V
- (2) $V_{DS} = 50$ V
- (3) $V_{DS} = 45$ V
- (4) $V_{DS} = 40$ V
- (5) $V_{DS} = 35$ V
- (6) $V_{DS} = 30$ V

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

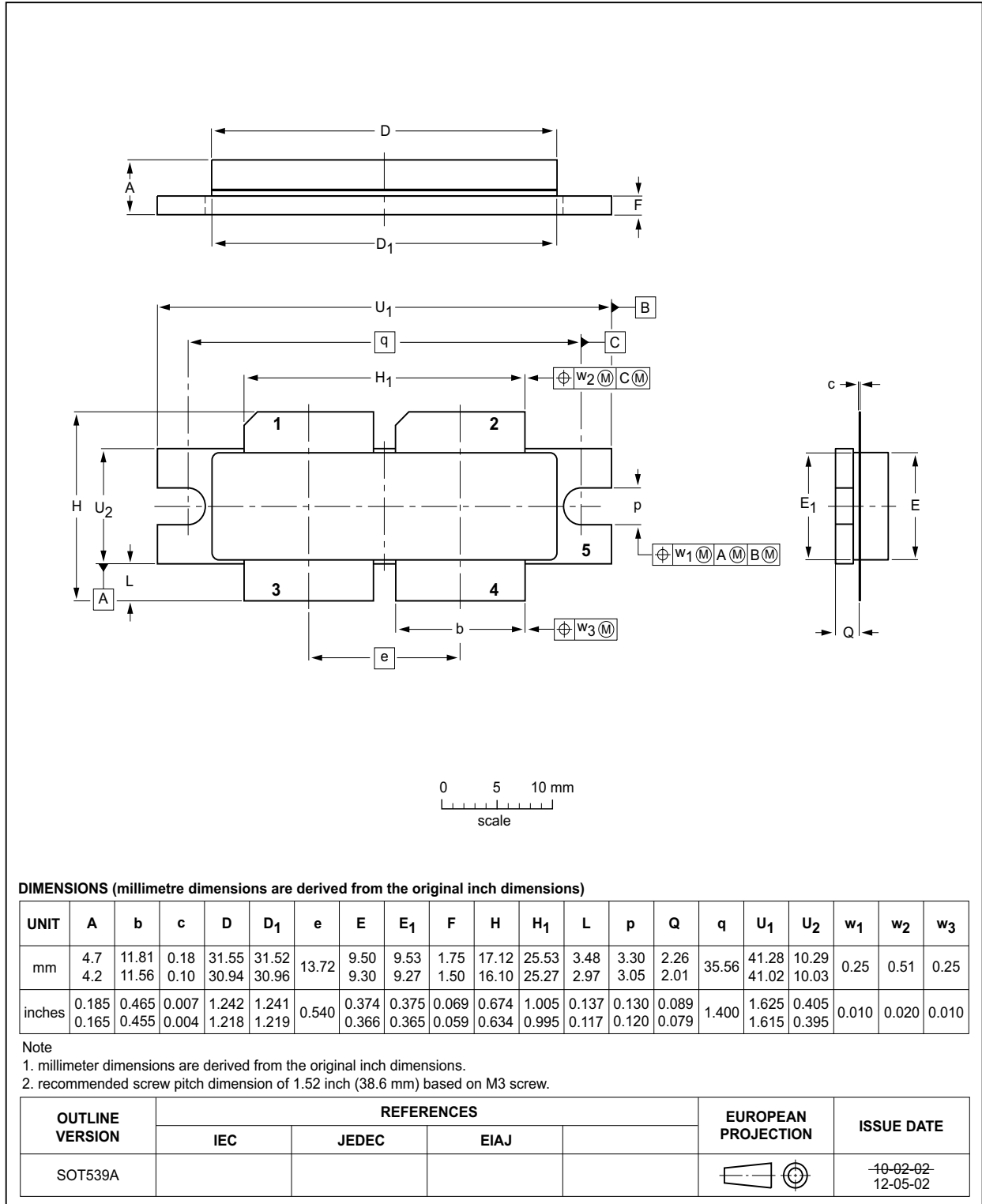


Fig 11. Package outline SOT539A

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
FM	Frequency Modulation
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MRI	Magnetic Resonance Imaging
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
UHF	Ultra High Frequency
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ART1K9FH v.2	20240327	Product data sheet	-	ART1K9FH v.1
Modifications:	<ul style="list-style-type: none"> Table 3 on page 2: corrected 12NC 			
ART1K9FH v.1	20240208	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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