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TRA_240_091 # EXB001

240-GHz Highly Integrated Radar Transceiver with Antenna on Chip

Preliminary Data Sheet

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Version Control

Revision	Changed section	Description of change	Reason for change
0.1		Generation of document	
0.2			

Table of Contents

1 Features

- Radar front end (RFE) with on-chip antenna
- Wide bandwidth of 45 GHz in frequency band of ISM band at 245 GHz
- Integrated low phase noise VCO
- Receiver with homodyne mixer
- Fully ESD protected device
- QFN 40 pin package, 5mm x 5mm with 0.4mm pitch, Pb-free, RoHS compliant
- IC is available as bare die, in package,
  on Radar Front End for evaluation with Evalkit Easy r4 and optionally with lens

1.1 Overview

The radar front end TRA_240_091 is an integrated transceiver circuit for 240-GHz operation with on-chip antenna. It includes a voltage-controlled oscillator, divide-by-8 frequency divider, an SPDT switch, a frequency multiplier-by-9 chain, frequency doublers, mixers, a low-noise amplifier, a power amplifier, antenna-coupler and integrated antenna (see Figure 1). For proper functionality, a lens must be placed on top of the chip. The lens can be provided by Silicon Radar.
The RF signal from the oscillator is amplified and fed to the frequency multiplier-by-9 chain and, and via a coupler to the integrated antenna. The RF signal from the oscillator is also directed to the RX path via amplifier and frequency doubler. The RX signal from the antenna is converted to baseband by a mixer with multiplied LO-signal.
The 13.5-GHz VCO has two analog tuning inputs with different tuning ranges and tuning slopes. Both tuning inputs have to be used to obtain the wide frequency tuning range of 45 GHz. The analog tuning inputs together with the integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With fixed oscillator frequency it can be used in continuous wave (CW) mode. Other modulation schemes are possible as well by utilizing the analog tuning inputs.
The IC is fabricated in SG13G2 SiGe BiCMOS technology of IHP GmbH.

1.2 Applications

The main field of application of the 240-GHz transceiver radar front end (RFE) is in short range radar systems which require high range resolution. 45 GHz of bandwidth theoretically gives a radar range resolution down to 6mm in air, and better than 6 mm for other materials with refractive index higher than one. The range resolution is inversely proportional to the refractive index of the material.
The maximum range depends on the gain of the lens that is used, and it can reach several meters. By using lenses with higher gain, the range can be increased.
The RFE can be used in FMCW mode as well as in CW mode.

2 Block Diagram

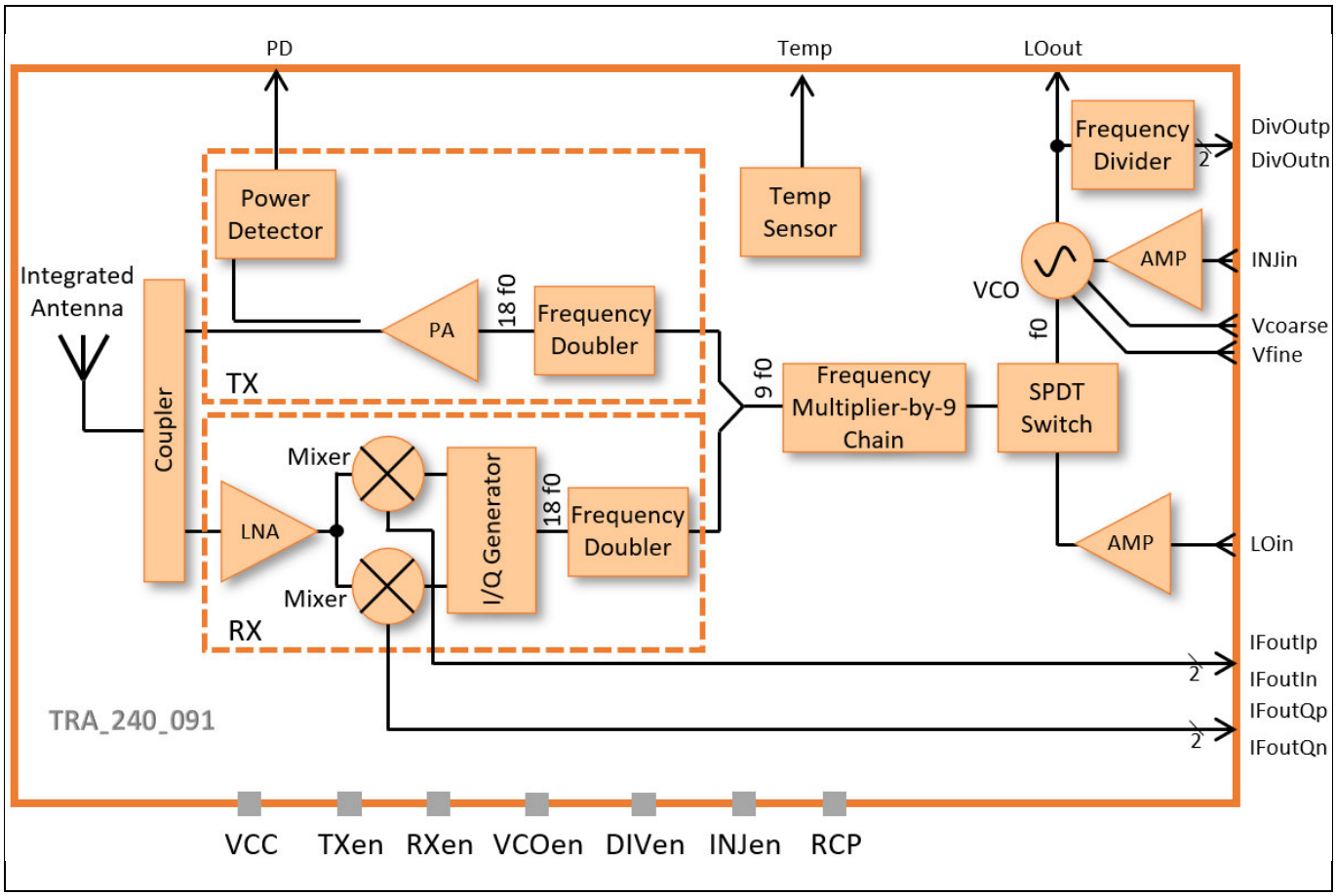


Figure 1 Block Diagram TRA_240_091

3 Pin Configuration

3.1 Pin Assignment

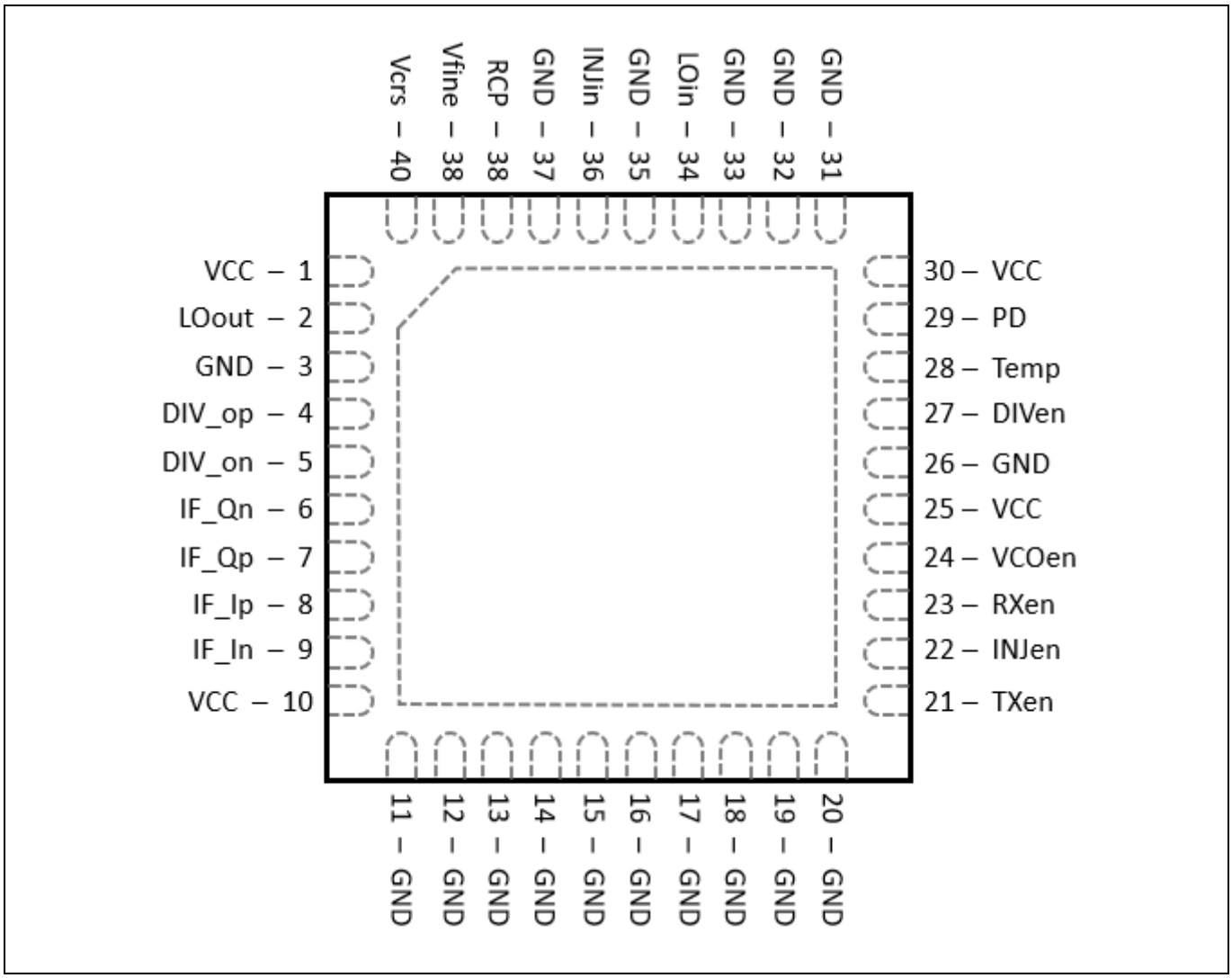


Figure 2 Pin Assignment (QFN, 5 mm × 5 mm)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	**Name**	
1,10,25,30	VCC	Global Supply: 3.3 V
2	LOout	VCO output RF-signal (single-ended 50ohm) (12-15 GHz)
4	DivOutp	Divider output (differential 100ohm) (3-3.75 GHz), DC-coupled, on-board dc-block capacitors are required
5	DivOutn	
6	IF_Qn	IF Q-output, DC-coupled ANALOG Output: DC-coupled low impedance might damage to circuit (> 500 Ω)
7	IF_Qp	
8	IF_Ip	IF I-output, DC-coupled ANALOG Output: DC-coupled low impedance might damage to circuit (> 500 Ω)
9	IF_In	

21	TXen	TX-blocks (TX120 GHz Amplifier, TX-Doubler, TX-PA) control pin DIGITAL: (3.3V for enable mode, 0V for disabled mode)
22	INJen	VCO's injection Amplifier control voltage, DIGITAL: (3.3V for enable mode, 0V for disabled mode)
23	RXen	RX-blocks (RX120 GHz Amplifier, RX-Doubler, RX-LNA, RX-IQ Mixers) control pin DIGITAL: (3.3V for enable mode, 0V for disabled mode)
24	VCOen	VCO&VCO's Buffer Amplifiers control voltage, DIGITAL: (3.3V for enable mode, 0V for disabled mode)
27	DIVen	Divider control voltage, DIGITAL: (3.3V for enable mode, 0V for disabled mode)
28	Temp	Temperature Sensor Output ANALOG Output: DC-coupled low impedance might damage to circuit. (> 500 Ω)
29	PD	TX-Power Detector Output ANALOG Output: Low impedance might damage to circuit. (> 500 Ω)
34	LOin	External LO input (single-ended 50ohm) (12-15 GHz)
36	INJin	12-15 GHz VCO injection input signal (single-ended 50ohm)
38	RCP	VCO Range control DIGITAL: (3.3V for 45 GHz, 0V for 23 GHz)
39	Vfine	Fine frequency tuning voltage of VCO, 0V to 3.3V, ANALOG.
40	Vcrs	Coarse frequency tuning voltage of VCO, 0V to 3.3V, ANALOG.
3,11-20,26, 31-33,35,37	GND	Global Ground. The IC's internal ground is connected to the exposed die attach pad of the QFN package. This pad must be soldered to PCB ground.

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the device may cause permanent damage to the device. Actual performance of the device is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Supply voltage Vcc	V_{CC}	-0.3	3.6	V	to GND
DC voltage at tuning inputs	V_t	-0.3	V_{CC} + 0.3	V	
DC voltage at enable inputs	V_{EN}	-0.3	V_{CC} + 0.3	V	
Junction temperature	T_J	-50	150	°C	
Storage temperature range	T_{STG}	-65	150	°C	
ESD robustness	V_{ESD}		tbd	kV	Human body model, HBM [1)]

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Ambient temperature	T_A	-40	65	°C	
Supply voltage Vcc	V_{CC2}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning input Vt	V_{Vt}	0	V_{CC}	V	
DC voltage at enable inputs	V_{EN}	0	V_{CC}	V	

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
Thermal resistance, junction-to-ambient	R_{thja}	-	-	tbd	K/W	JEDEC Standard JESDxx-x

4.4 Electrical Characteristics

T_A = -40 °C to +65 °C unless otherwise noted. Typical values measured at T_A = 25 °C and V_{CC} = 3.3 V.

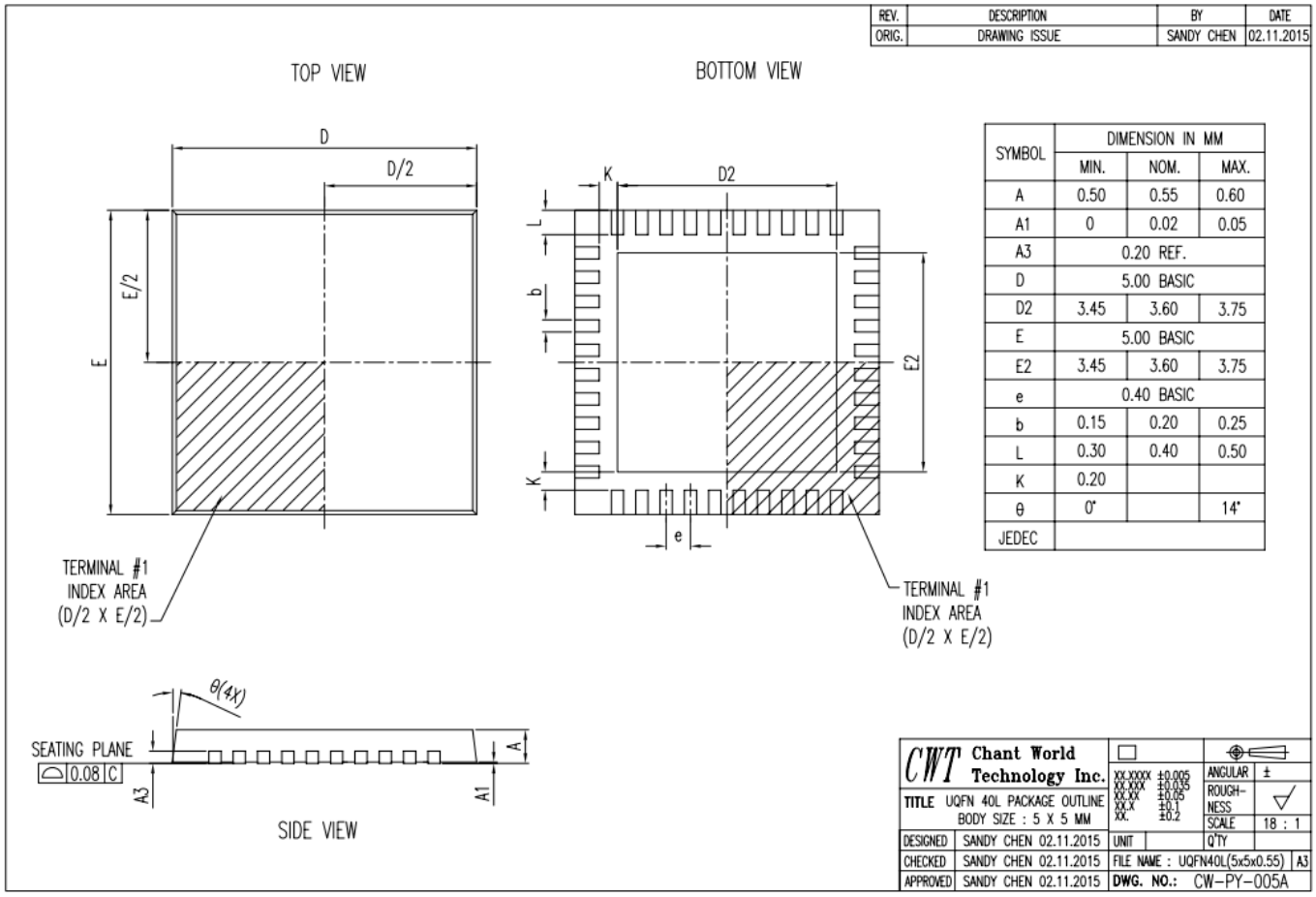
Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
DC Parameters						
Supply current consumption at V_{CC1}	I_{CC1}	tbd	260	tbd	mA	
Enable input voltage, low level	V_{EN_L}	0		0.3	V	
Enable input voltage, high level	V_{EN_H}	2.7	3.3	V_{CC}	V	

VCO tuning voltage	V_{Vt}	0		V_{CC}	V	
RF Parameters						
Start frequency	f_{TX}	tbd	222.5	tbd	GHz	
Stop frequency	f_{TX}	tbd	267.5	tbd	GHz	
Tuning full bandwidth	Δf_{TX}	tbd	45	tbd	GHz	
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		Tbd		MHz/V	
Phase noise	P_N	tbd	-110	tbd	dBc/Hz	at 1 MHz offset, LOout
Transmitter output power	P_{TX}	tbd	2	tbd	dBm	
Divider ratio of TX signal	N_{div}		72			
Divider output power	P_{div}	tbd	-5	tbd	dBm	
Divider output start frequency	f_{div}	tbd	2.80	tbd	GHz	
Divider output stop frequency		tbd	3.75	tbd	GHz	
Receiver gain	g_{RX}	tbd	18	tbd	dB	
IF frequency range	f_{IF}	0		100	MHz	
IF output impedance	Z_{OUT}		500		Ω	Differential outputs
IQ amplitude imbalance	Aimb	tbd	1	tbd	dB	
IQ phase imbalance	PHimb	tbd	4	tbd	deg	
Noise figure (DSB)	NF	tbd	15.7	tbd	dB	
Input compression point	1dB ICP	tbd	-16.5	tbd	dBm	

5 Packaging

5.1 Outline Dimensions



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.20 REF.	
D		5.00 BASIC	
D2	3.45	3.60	3.75
E		5.00 BASIC	
E2	3.45	3.60	3.75
e		0.40 BASIC	
b	0.15	0.20	0.25
L	0.30	0.40	0.50
K	0.20		
θ	0°		14°
JEDEC			

Figure 3 Outline Dimensions of QFN40 Package with Exposed Pad

5.2 Package Code

Top-Side Markings TRA091
YYWW

5.3 Antenna Position

The position of the radiating center of the integrated antenna is 500um off the center of the 5 x 5 mm² package.

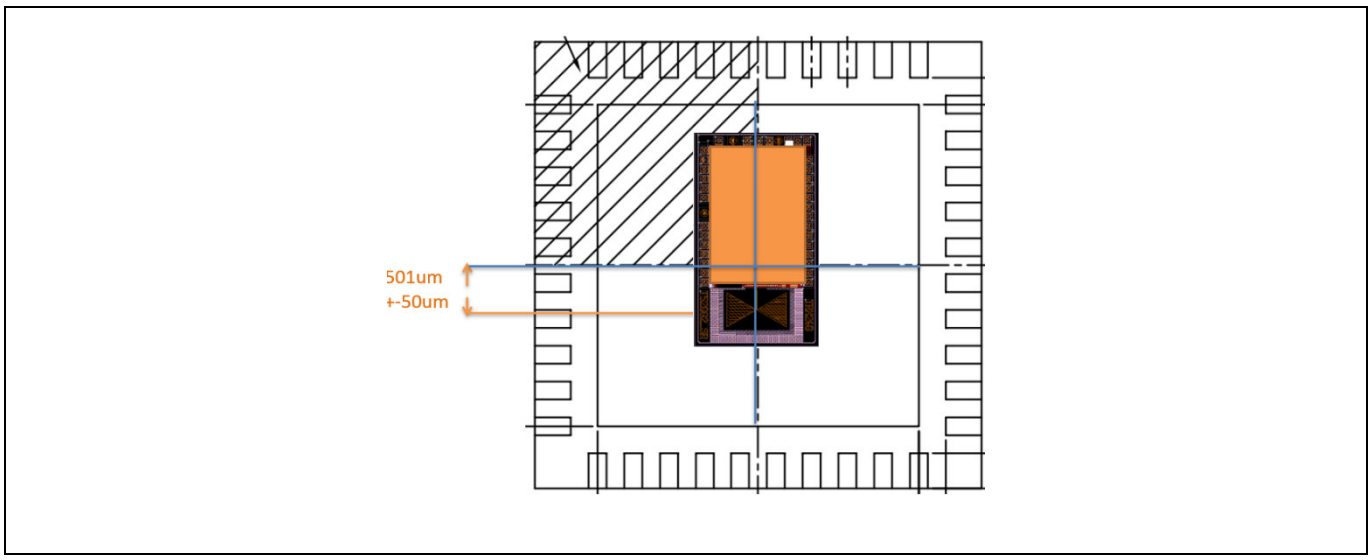


Figure 11 Antenna center vs. package center

6 Application

6.1 Application Circuit Schematic

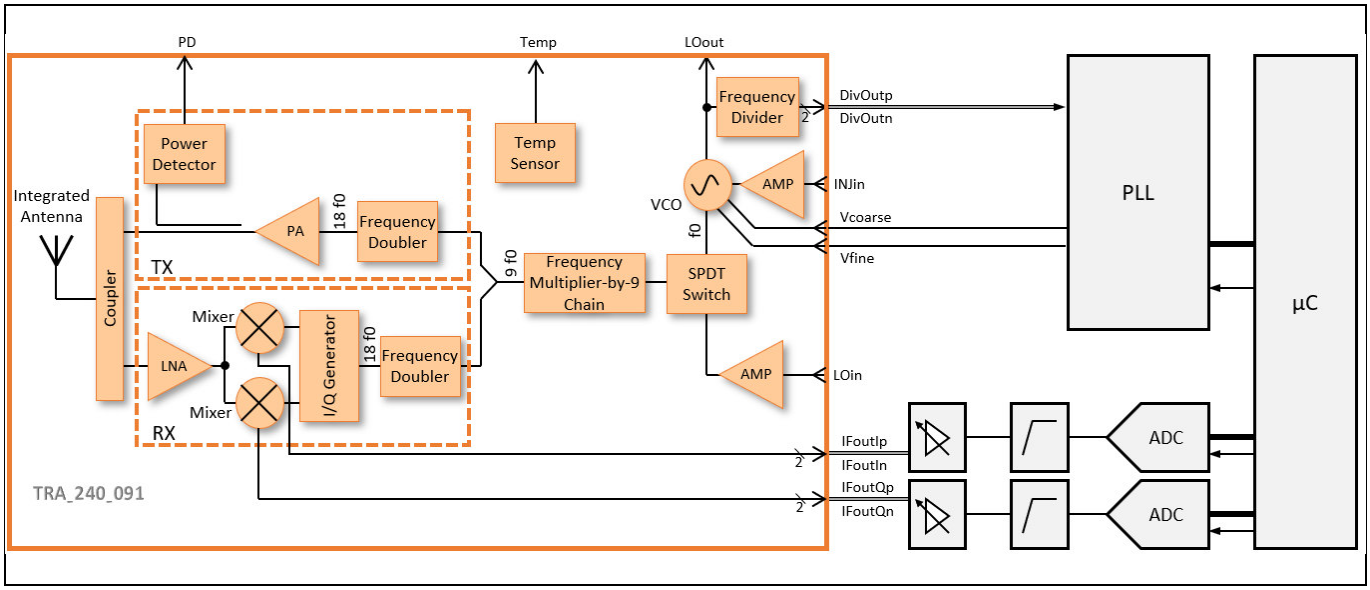


Figure 4 Suggested application circuit

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 µs and 100 µs is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Kit

Silicon Radar offers evaluation kits for speeding up radar development. Please review our website and product sheets for more information: https://www.siliconradar.com/evalkits/.
The *SiRad Easy® r4* platform supports development for many of Silicon Radar's integrated IQ transceivers including radar front end boards for TRA_240_091. It serves as reference hardware and provides a design environment including a graphical user interface for parameter setting. Its functionality and communication protocol are adaptable to development projects.

6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that voltages applied to the input pins should never exceed the related V_{CC} by more than 0.3 V. Otherwise, supply current may be sourced through upper ESD protection diodes connected at the pin.
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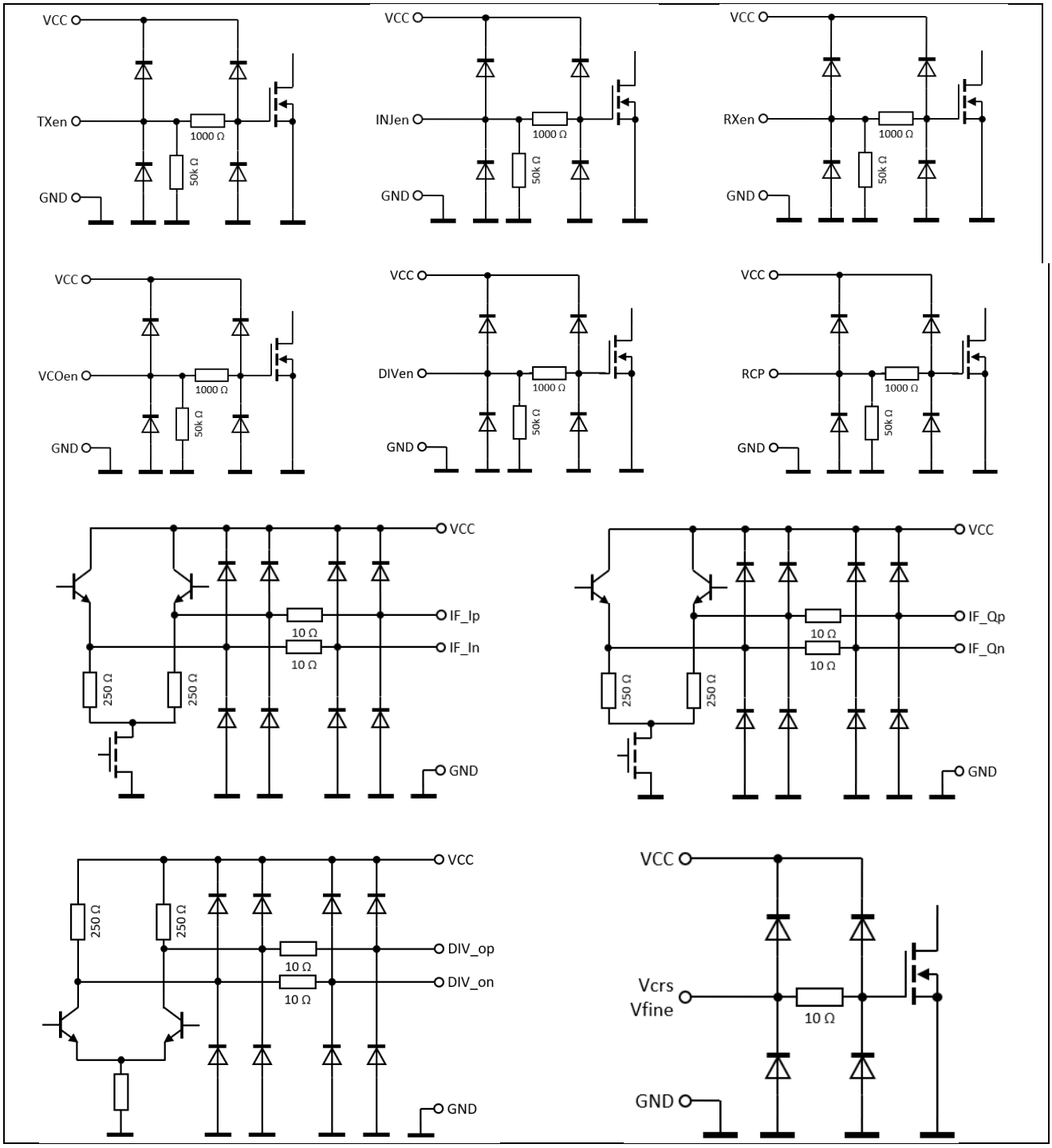

Figure 10 Equivalent I/O circuits

7 Reliability and Environmental Test

Table 6 Reliability and Environmental Test according to JEDEC Standards

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	tbd
Temperature Cycling	JESD22-A104	850 cycles at -40°C … 125°C	tbd
HTSL	JESD22-A103	1,000 h at 150°C	tbd
HTOL	JESD22-A108	1,000 h at 85°C	tbd
THB	JESD22-A101	1,000 h at 85°C and 85% RH	tbd

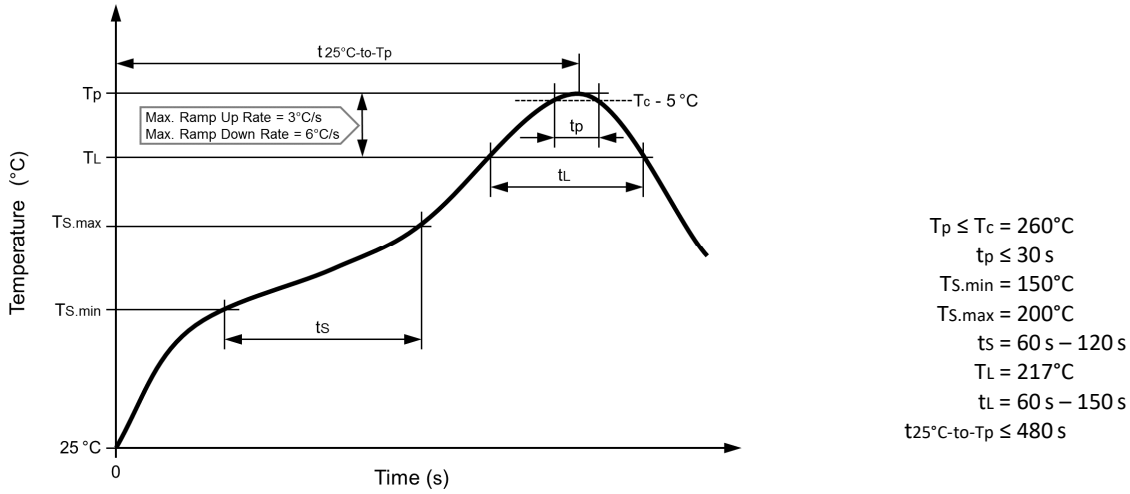

Figure 5 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

8 Measurement Results

Will be provided at later state as test campaigns are completed.

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